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[List of Attachment]

[Attachment] Specification 1

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[Name of Document] Specification

[Title of the Invention] A LIGHT EMITTING DEVICE AND A MANUFACTURING METHOD THEREOF

[Scope of Claim]

[Claim 1]

A light emitting device characterized by comprising an n-channel TFT and a light emitting element in a pixel, the n-channel TFT comprising:

an active layer including:

a channel forming region;

an n-type impurity region (c) adjacent to the channel forming region;

an n-type impurity region (b) adjacent to the n-type impurity region (c); and

an n-type impurity region (a) adjacent to the n-type impurity region (b); and

a gate electrode including:

a first gate electrode; and

a second gate electrode an external form of which is smaller than that of the first gate electrode,

wherein the first gate electrode overlaps the channel forming region and the n-type impurity region (c) with the gate insulating film interposed therebetween; and

wherein the second gate electrode overlaps the channel forming region with the gate insulating film interposed therebetween.

[Claim 2]

A light emitting device characterized by comprising a driver circuit comprising an n-channel TFT, and a pixel portion comprising a light emitting element, the n-channel TFT comprising:

an active layer including:

a channel forming region;

an n-type impurity region (c) adjacent to the channel forming region;

an n-type impurity region (b) adjacent to the n-type impurity region (c); and

an n-type impurity region (a) adjacent to the n-type impurity region (b); and

a gate electrode including:

a first gate electrode; and

a second gate electrode an external form of which is smaller than that of the first gate electrode,

wherein the first gate electrode overlaps the channel forming region and the n-type impurity region (c) with the gate insulating film interposed therebetween, and

wherein the second gate electrode overlaps the channel forming region with the gate insulating film interposed therebetween.

[Claim 3]

The light emitting device according to claim 1 or claim 2, characterized in that the first gate electrode is formed of tantalum nitride or titanium nitride, and the second gate electrode is formed of tungsten or an aluminum alloy.

[Claim 4]

The light emitting device according to any one of claims 1 to 3, characterized in that the n-type impurity region (a) contains an n-type impurity element at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3, the n-type impurity region (b) contains an n-type impurity element at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3, and the n-type impurity region (c) contains an n-type impurity element at a concentration of 1×10^{16} to 1×10^{18} atoms/cm^3.

[Claim 5]

The light emitting device according to claims 1 to 4, characterized in that the gate electrode is covered by an insulating film in which a resin film and one of a silicon nitride film and a silicon nitride oxide film are laminated.

[Claim 6]

The light emitting device according to claim 5, characterized in that a coloring layer is provided on one of the silicon nitride film and the silicon nitride oxide film, and the resin film is provided so as to cover the coloring layer.

[Claim 7]

A method of manufacturing a light emitting device characterized by comprising:

a first step of forming a semiconductor film on an insulator;

a second step of forming an insulating film covering the semiconductor film;

a third step of forming a conductive film on the insulating film by laminating two or more conductive films;

a fourth step of forming a gate electrode by etching the conductive film;

a fifth step of adding an n-type impurity element to the semiconductor film by using the gate electrode as a mask;

a sixth step of etching a side face of the gate electrode and then selectively etching a portion of the gate electrode;

a seventh step of adding an n-type impurity element to the semiconductor film through a portion of the gate electrode using as a mask a portion in which two or more conductive films of the gate electrode are laminated after the sixth step;

an eighth step of forming an insulating film covering the gate electrode;

a ninth step of forming a wiring on the insulating film formed in the eighth step to be in contact with the semiconductor film; and

a tenth step of forming a light emitting element on the insulating film formed in the eighth step.

[Claim 8]

The method of manufacturing a light emitting device according to claim 7, characterized in that the conductive film is formed by laminating one of a tungsten film and an aluminum alloy film on one of a tantalum nitride film and a titanium nitride film.

[Claim 9]

The method of manufacturing a light emitting device according to claim 7, characterized in that the gate electrode formed in the fourth step is formed to have a tapered side.

[Claim 10]

A method of manufacturing a light emitting device characterized by comprising:

a first step of forming a semiconductor film on an insulator;

a second step of forming an insulating film covering the semiconductor film;

a third step of forming a conductive film on the insulating film by laminating

a first conductive film and a second conductive film;

a fourth step of forming a first gate electrode comprising the first conductive film and a second gate electrode comprising the second conductive film by etching the conductive film;

a fifth step of adding an n-type impurity element to the semiconductor film by using the first gate electrode and the second gate electrode as a mask;

a sixth step of etching the first gate electrode and the second gate electrode to thin widths and then selectively etching the second gate electrode;

a seventh step of adding an n-type impurity element to the semiconductor film through a portion of the first gate electrode using the second gate electrode as a mask after the sixth step;

an eighth step of forming an insulating film covering the gate electrode ;

a ninth step of forming a wiring on the insulating film formed in the eighth step to be in contact with the semiconductor film; and

a tenth step of forming a light emitting element on the insulating film formed in the eighth step.

[Claim 11]

The method of manufacturing a light emitting device according to claim 10, characterized in that one of a tantalum nitride film and a titanium nitride film is used as the first conductive film, and one of a tungsten film and an aluminum alloy film is used as the second conductive film.

[Claim 12]

The method of manufacturing a light emitting device according to claim 10, characterized in that each of the first gate electrode and the second gate electrode formed in the fourth step is formed to have a tapered side.

[Claim 13]

The method of manufacturing a light emitting device according to any one of claims 7 to 12, characterized in that the insulating film formed in the eighth step includes a coloring layer.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention]

The present invention relates to a light emitting device which has an element with a luminescent material put between electrodes and an electronic appliance using the light emitting device for a display portion (a display or a displaying monitor), particularly to a light emitting device using a luminescent material by which EL (Electro Luminescence) can be obtained (hereinafter referred to as an EL material).

[0002]

[Prior Art]

Recently, there has been a proceeding development of light emitting devices (hereinafter referred to as EL light emitting devices) using self-light emitting elements (hereinafter referred to as EL elements) utilizing EL phenomenon of luminescent materials. The EL light emitting devices, being display devices using self-light emitting elements, require no backlight as in liquid crystal display devices. Furthermore, with their wide viewing angles, the EL light emitting devices attract attention as displays of portable devices used outdoors.

[0003]

There are two types of the EL light emitting devices, i.e. an active matrix type and a passive matrix type. There has been a development of both types actively carried out. At present, the active matrix type EL light emitting device is particularly attracting attention. The active matrix type EL light emitting device is characterized in that a thin film transistor (hereinafter referred to as a TFT) is provided for each of pixels of a pixel portion to control an amount of current flowing to an EL element.

[0004]

The advantage of the active matrix type is that a highly fine image can be displayed and an image with larger amount of information can be provided.

[0005]

However, providing the TFT for each of the pixels makes a manufacturing process more complicated, and there are problems in reduction in yield and increase in manufacturing cost due to a protracted manufacturing term. In particular, many

photolithography steps cause a remarkable reduction in yield, so a reduction in the number of photolithography steps is an important subject.

[0006]

[Problems to be Solved by the Invention]

The invention is made in view of the above-mentioned problems, to provide an inexpensive light emitting device by reducing the number of photolithography steps to improve yield, shorten manufacturing term and reduce manufacturing cost. In addition, it is another object of the invention to provide an inexpensive electronic appliance in which an inexpensive light emitting device is used as a display portion.

[0007]

[Means for Solving the Problem]

According to the invention, the number of photolithography steps in relation to manufacturing the TFT is reduced to improve yield of the light emitting device and shorten a manufacturing term thereof. Features of the invention are that a gate electrode is formed of a plurality of layers of conductive films of which selectivity in etching is used for adjusting a concentration of an impurity region formed in an active layer.

[0008]

An example of a typical manufacturing step of an n-channel TFT which characterizes the invention is explained with reference to FIG. 1. In FIG. 1A, reference numeral 100 denotes an insulator, which is a substrate provided with an insulating film thereon, an insulating substrate, or an insulating film. On the insulator 100, a semiconductor film (typically a silicon film) 101 is formed which becomes an active layer of the TFT. The semiconductor film 101 is covered with an insulating film 102 containing silicon, which becomes a gate insulating film of the TFT. Note that for the insulating film containing silicon, a silicon oxide film, a silicon nitride film, a silicon nitride oxide film, or a laminated film of combination of them can be used.

[0009]

Next, on the insulating film 102 containing silicon, a first conductive film 103 and a second conductive film 104 are formed. Here, it is important that the first

conductive film 103 and the second conductive film 104 are allowed to have selectivity to each other in etching. Specifically, it can also be said that it is important that there is an etching condition that the second conductive film 104 can be etched with the first conductive film 103 remaining.

[0010]

Typical combinations are 1) the combination of a tantalum nitride film as the first conductive film and a tungsten film as the second conductive film, 2) the combination of a tungsten film as the first conductive film and an aluminum film as the second conductive film, or 3) the combination of a titanium nitride film as the first conductive film and a tungsten film as the second conductive film.

[0011]

In the above combination of 1), the tungsten film and the tantalum nitride film are etched by a combination of chlorine (Cl_2) gas and carbon tetrafluoride (CF_4) gas. By adding oxygen (O_2) gas to the gasses, an etching rate of the tantalum nitride film is extremely reduced, thereby selectivity can be obtained.

[0012]

Moreover, in the above combination of 2), with the combination of bromine trichloride ($BrCl_3$) gas and chlorine (Cl_2) gas, an aluminum film is etched and a tungsten film is not etched. Furthermore, with the combination of chlorine (Cl_2) gas and carbon tetrafluoride (CF_4) gas, a tungsten film is etched, but an aluminum film is not etched. In this way, selectivity can be provided for both of the conductive films.

[0013]

Next, as shown in FIG. 1B, the first conductive film 103 and the second conductive film 104 are etched by using a resist mask 105 to form a gate electrode 106. Here, a gate electrode obtained by etching the first conductive film is to be referred to as a first gate electrode, and a gate electrode obtained by etching the second conductive film is to be referred to as a second gate electrode. Therefore, the gate electrode 106 comprises the first electrode 106a and the second gate electrode 106b.

[0014]

The gate electrode 106 is preferably formed in a shape with a taper by an

etching condition. A taper is a portion that an edge face at an edge portion of an electrode is inclined. An angle between the edge face and the base film is referred to as a tapered angle. To be formed in a shape with taper is that the electrode is formed in a shape with edges each being inclined with a tapered angle. A trapezoid is included in a tapered shape.

[0015]

In forming the gate electrode 106, the gate insulating film 102 is also etched slightly to be a little thinned. The thinning is preferably suppressed within 20 to 50 nm although it depends on etching conditions.

[0016]

In this state, an impurity element (hereinafter referred to as an n-type impurity element) is added into the semiconductor film 101 for making the semiconductor an n-type semiconductor. At this time, the gate electrode 106 is used as a mask to add the n-type impurity element to the semiconductor film 101 in a self-aligned manner. As a specific n-type impurity element, an element which belongs to group fifteen in the periodic table (typically phosphorus or arsenic) can be used.

[0017]

A well-known plasma doping method or an ion implantation method can be used as the adding method at this time. The impurity element can be added to the semiconductor film at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3. Each of regions 107 and 108 which is added an n-type impurity element at such a concentration is referred to as an n-type impurity region (a) in this specification.

[0018]

Next, as shown in FIG. 1C, the gate electrode 106 is further etched under the same condition as that in forming the gate electrode 106. Then a gate electrode 109 is formed with further thinned width (the gate electrode 109 comprises a first gate electrode 109a and a second gate electrode 109b). At this time, there is a progress in thinning of the gate insulating film 102.

[0019]

Next, when the etching step shown in FIG. 1C is carried out, the etching

condition is changed so as to allow the second gate electrode 109b to be selectively etched. Parameters such as the etching gas, substrate bias voltage, and electric power applied to electrodes may be changed. Here, since it is necessary only to secure selectivity between the first gate electrode 109a and the second gate electrode 109b, the easiest way therefore is to change the etching gas.

[0020]

Thus, as shown in FIG. 1D, a gate electrode 111 which comprises a laminated structure of the first gate electrode 109a and a second gate electrode 110 is formed.

[0021]

In this state, an adding step of the n-type impurity element is carried out again. This adding step is carried out with a higher acceleration voltage than that in the step shown in FIG. 1B so that the impurity element can reach deep position. At this time, regions denoted by reference numerals 112 and 113 are doped with an n-type impurity element at a concentration of 1×10^{17} to 1×10^{19} atoms/cm^3. Each of the regions 112 and 113 which is added the n-type impurity element at such a concentration is to be referred to as an n-type impurity region (b) in this specification.

[0022]

Moreover, regions denoted by reference numerals 114 and 115 are also added the n-type impurity element each through an end portion of the first gate electrode 109a (a portion without being in contact with the second gate electrode 110). Therefore, a concentration of the n-type impurity element in the regions 114 and 115 is lower than that in the n-type impurity region (b) (preferably 1×10^{16} to 1×10^{18} atoms/cm^3). Each of the regions 114 and 115 which is added the n-type impurity element at such a concentration is to be referred to as an n-type impurity region (c).

[0023]

A region 116 which is not added the n-type impurity element is a region which functions as a channel forming region of the TFT, and is formed directly below the gate electrode 110.

[0024]

After this, as shown in FIG. 1E, a passivation film 117, an interlayer

insulating film 118, a source wiring 119 and a drain wiring 120 are formed to complete formation of the n-channel TFT. As the passivation film 117, a silicon nitride film or a silicon nitride oxide film can be used. As the interlayer insulating film 118, an inorganic insulating film, an organic insulating film, or a lamination film of them can be used. A resin film such as polyimide, an acrylic resin, polyamide, or BCB (benzocyclobutene) can be used as the organic insulating film. Further, as the source wiring 119 and the drain wiring 120, known conductive films can be used.

[0025]

In the above manufacturing steps, there are only four photolithography steps, which are carried out when the semiconductor film 101 is formed, the gate electrode 106 is formed, contact holes in the interlayer insulating film are formed, and the source wiring and the drain wiring are formed. In forming a CMOS circuit, an additional photolithography step is required for manufacturing a p-channel TFT. Nevertheless, this requires only five photolithography steps.

[0026]

The TFT shown in FIG. 1E has the n-type impurity region (b) 113 and the n-type impurity region (c) 115 which are formed between the channel forming region 116 and the drain region 108. Here, the n-type impurity region (c) 115 and the first gate electrode 109a overlap with the gate insulating film 102 interposed therebetween. This structure is very effective in preventing hot carrier deterioration. Moreover, the n-type impurity region (b) 113 is a region which behaves similarly to a conventional LDD (Light-Doped Drain) region.

[0027]

Therefore, in the TFT shown in FIG. 1E, it is a measure for preventing hot carrier to provide the n-type impurity region (c) and it is a measure for preventing leak current to provide the n-type impurity region (b). Accordingly, a structure with a significantly high reliability is provided. Such a highly reliable TFT can be manufactured through only five photolithography steps. This makes it possible not only to improve yield and shorten the manufacturing term of the whole light emitting device including light emitting elements but also to manufacture an inexpensive and

highly reliable light emitting device.

[0028]

Explanation of data

[0029]

[Embodiment Modes of the Invention]

Embodiment modes of the invention is explained in detail using embodiments shown below.

[0030]

[Embodiment 1]

An embodiment of the invention is explained with reference to FIG. 2 to FIG. 4. Here, an explanation is made on a method of simultaneously manufacturing a TFT of a pixel portion and a TFT of a driver circuit provided in the periphery of the pixel portion. For simplifying the explanation, a CMOS circuit as a basic unit of the circuit is shown with respect to the driver circuit.

[0031]

First, as shown in FIG. 2A, a base film 302 is formed in thickness of 300 nm on a glass substrate 301. In this embodiment, silicon oxynitride films are laminated to be used as the base film 302. At this time, a nitrogen concentration in the base film 302 on the side in contact with the glass substrate 301 is preferably 10 to 25 wt%.

[0032]

It is effective for the base film 302 to be provided with a heat radiation effect. Thus, it is effective to provide a carbon film, in particular a DLC (Diamond-Like Carbon) film, on both or one side of the substrate 301. The DLC film can be deposited by a CVD method or a sputtering method, and has an advantage in that the deposition is possible at a temperature ranging from a room temperature to 100°C.

[0033]

Next, on the base film 302, an amorphous silicon film (not shown) is formed in thickness of 50 nm by a known deposition method. The film is not limited to the amorphous silicon film, and may be a semiconductor film which has an amorphous structure (including a microcrystalline semiconductor film). Furthermore, a compound

semiconductor film including the amorphous structure such as an amorphous silicon germanium film may be used as well. The film thickness may be 20 to 100 nm.

[0034]

Then, an amorphous silicon film is crystallized by a method disclosed in Japanese Patent Laid-Open No. 7-130652 to form a crystalline silicon film (referred to as a polycrystalline silicon film or a polysilicon film) 303. In this embodiment, nickel is used as an element for promoting crystallization. It is needless to say that a laser annealing crystallization method using laser light or a lamp annealing crystallization method using infrared light can be used as other methods for crystallization.

[0035]

Next, as shown in FIG. 2B, the crystalline silicon film 303 is etched by a first photolithography step to form island-like semiconductor films 304 to 307, which become active layers of TFTs later.

[0036]

Here, in this embodiment, a protection film (not shown) formed of a silicon oxide film is formed in thickness of 130 nm on the semiconductor films 304 to 307. The semiconductor films 304 to 307 are then added an impurity element that makes the semiconductor a p-type semiconductor (hereinafter referred to as a p-type impurity element). An element which belongs to the group thirteen of the periodic table (typically boron or gallium) can be used as the p-type impurity element. This protection film is provided for protecting the crystalline silicon films so as not to be directly exposed to plasma and for allowing a subtle control of the concentration.

[0037]

The concentration of the p-type impurity element added at this time can be 1×10^{15} to 5×10^{17} atoms/cm^3 (typically 1×10^{16} to 1×10^{17} atoms/cm^3). The p-type impurity element added at this concentration is used for adjusting a threshold voltage of the n-channel TFT.

[0038]

Then, a gate insulating film 308 is formed covering the semiconductor films 304 to 307. As the gate insulating film 308, an insulating film containing silicon can

be used in thickness of 10 to 200 nm, preferably 50 to 150 nm. The gate insulating film 308 can take either of a single layer structure and a lamination structure. In this embodiment, a silicon nitride oxide film in thickness of 115 nm is used.

[0039]

Next, a tantalum nitride film of in thickness of 30 nm is formed as a first conductive film 309 and further a tungsten film in thickness of 370 nm is formed as a second conductive film 310. These metal films can be formed by a sputtering method. Addition of inert gas such as Xe and Ne as a sputtering gas can prevent separation of the film due to stress. In addition, by using a tungsten target with a purity of 99.9999%, a low resistant tungsten film can be formed with a resistivity of 20 mΩcm or lower.

[0040]

Then, resist masks 311a to 311g are formed for etching the first conductive film 309 and the second conductive film 310. The etching treatment carried out here is called first etching treatment in this specification.

[0041]

In this embodiment, an etching method using ICP (Inductively Coupled Plasma) is employed. A mixed gas of carbon tetrafluoride (CF_4) gas and chlorine (Cl_2) gas is used with a deposition pressure of 1 Pa. In this state, plasma is generated with 500 W of RF power (13.56 MHz) applied to a coil-shaped electrode. In addition, 150 W of RF power (13.56 MHz) is applied to a stage on which the substrate mounted as a self-bias voltage so that a negative self-bias voltage is applied to the substrate.

[0042]

The etching treatment carried out under such a condition provides selectivity of the tantalum nitride film and the tungsten film nearly 1 : 1, which makes it possible to etch them together. Furthermore, by making use of retreat of the edges of the resist masks 311a to 311e, the first conductive film 309 and the second conductive film 310 can be etched in a tapered shape with a tapered angle of 15 to 45°. With the etching condition of this embodiment, a tapered angle of about 25° can be obtained.

[0043]

Thus, gate electrodes 312 to 316, each formed of a lamination film

comprising the first conductive film and the second conductive film, and a source wiring 317 and a drain wiring 318 of a switching TFT are formed. Here, the drain wiring 318 also functions as a gate electrode of a current controlling TFT.

[0044]

Next, with the gate electrodes 312 to 316, the source wiring 317, and the drain wiring 318 used as masks, an n-type impurity element (in this embodiment, phosphorus) is added in a self-aligned manner. In thus formed impurity regions 319 to 327, the n-type impurity element is contained at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3 (typically 2×10^{20} to 5×10^{21} atoms/cm^3). The impurity regions 319 to 327 form source regions and drain regions of n-channel TFTs.

[0045]

Next, the gate electrodes are etched using the resist masks 311a to 311g. The etching condition at this time can be the same as that in the first etching treatment. Here, the tapered part of each of the gate electrodes is made to retreat. Accordingly, gate electrodes 328 to 332, a source wiring 333, and a drain wiring 334 are formed each of which has a thinner width than that shown in FIG. 2C.

[0046]

Furthermore, as shown in FIG. 2E, the second conductive films (tungsten films) are selectively etched using the resist masks 311a to 311g. The etching condition thereof is to mix oxygen gas in the etching gas of the first etching treatment. The etching treatment carried out here is to be referred to as second etching treatment. This is because mixing oxygen gas in the etching gas makes progress of etching of the first conductive film (tantalum nitride film) extremely slow.

[0047]

At this time, gate electrodes 335 to 339 having laminated structures comprising first gate electrodes 335a to 339a and second gate electrodes 335b to 339b are formed respectively. Further, a source wiring 340 having a laminated structure comprising a first source wiring 340a and a second source wiring 340b, and a drain wiring 341 having a laminated structure comprising a first drain wiring 341a and a second drain wiring 341b are formed.

[0048]

Next, the resist masks 311a to 311g are removed, and an n-type impurity element (in this embodiment, phosphorus) is added as shown in FIG. 3A. In this step, adjustment is made so that the n-type impurity element is contained in each of n-type impurity regions 342 to 351 at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3 (typically 5×10^{17} to 5×10^{18} atoms/cm^3). The impurity region which is added the n-type impurity element at the above concentration is to be referred to as the n-type impurity region (b) in this specification.

[0049]

At this time, n-type impurity regions 352 to 361 are formed simultaneously. These impurity regions are formed by the n-type impurity element which have passed through the first gate electrodes 335a to 339a, therefore, phosphorus is added at a concentration of 1/2 to 1/10 (typically, 1/3 to 1/4) of those in the n-type impurity regions 342 to 351. Specifically, the n-type impurity element is contained at a concentration of 1×10^{16} to 5×10^{18} atoms/cm^3 (typically 3×10^{17} to 3×10^{18} atoms/cm^3). The impurity region which is added the n-type impurity element at the above concentration is to be referred to as the n-type impurity region (c) in this specification.

[0050]

It is necessary to add the n-type impurity element through the first gate electrodes 353a to 339a and the gate insulating film 308. Therefore, an acceleration voltage is set a little higher, which is 70 to 120 kV (in this embodiment, 90 kV).

[0051]

Next, as shown in FIG. 3B, a resist mask 362 is formed. Then, a p-type impurity element (in this embodiment, boron) is added to form impurity regions 363 to 366 containing a high concentration of boron. Here, by the ion doping method using diborane (B_2H_6), boron is added so that the concentration thereof becomes 3×10^{20} to 3×10^{21} atoms/cm^3 (typically 5×10^{20} to 1×10^{21} atoms/cm^3). The acceleration voltage can be 20 to 30 kV. The impurity region which is added the p-type impurity element at the above concentration is to be referred to as the p-type impurity region (a) in this specification.

[0052]

Each of the p-type impurity regions (a) 363 to 366 includes a region already added phosphorus at a concentration of 1×10^{20} to 1×10^{21} atoms/cm^3. Here, however, boron is added at a concentration at least three times as high or higher as phosphorus. Therefore, the already formed n-type impurity regions are completely reversed to p-type to function as p-type impurity regions.

[0053]

Next, the resist mask 362 is removed before forming a protection film (not shown) formed of a silicon nitride film or a silicon nitride oxide film. Then, the n-type or p-type impurity element added at respective concentrations is activated. As means for activating in this embodiment, a furnace annealing method is employed, and heat treatment is carried out in an electric furnace in a nitrogen atmosphere at 550°C for four hours. At this time, it is desirable to keep an oxygen concentration in the nitrogen atmosphere as low as possible. This is for preventing the gate electrodes from being oxidized. The oxygen concentration is preferably 1 ppm or lower.

[0054]

At this time, nickel atoms used for crystallizing the amorphous silicon film move in directions of arrows to the regions which are added the n-type impurity element, namely the n-type impurity regions or the p-type impurity regions containing the n-type impurity element, and then gettered. That is, the nickel concentration in channel forming regions 367 to 371 of the TFTs is considerably reduced to at most 1×10^{16} atoms/cm^3 or lower (though this value is a measurable lower limit of the mass secondary ion analysis).

[0055]

Further, a protecting film 372 formed of a silicon nitride film or a silicon nitride oxide film is formed before heat treatment at a temperature ranging from 300 to 450°C in a nitrogen atmosphere to perform hydrogenation treatment. This step is performed to terminate dangling bonds of the semiconductor by thermally excited hydrogen atoms. In this treatment, hydrogen contained in the protecting film 372

diffuses to perform the hydrogenation treatment. Besides, plasma hydrogenation treatment can be carried out.

[0056]

The hydrogenation treatment can also be carried out by performing heat treatment at 300 to 450°C for 1 to 12 hours in an atmosphere containing 3 to 100% of hydrogen.

[0057]

Then, as shown in FIG. 3D, a coloring layer 373 is formed in a thickness of 0.3 to 2 μm by a printing method, a spin coating method, or an ink-jetting method. As the coloring layer 373, a resin film containing a pigment can be used. Here, the coloring layer 373 is formed before openings 374a to 374i are formed. These openings are formed for removing the coloring layer beforehand at portions where contact holes are to be formed later.

[0058]

For the coloring layer 373, a coloring layer which transmits light with a peak at a wavelength of approximately 650 nm (hereinafter referred to as a red coloring layer), a coloring layer which transmits light with a peak at a wavelength of approximately 550 nm (hereinafter referred to as a green coloring layer), or a coloring layer which transmits light with a peak at a wavelength of approximately 450 nm (hereinafter referred to as blue coloring layer) can be used. It is needless to say that coloring layers which transmit light of other colors can be used as well.

[0059]

In order to obtain as much light as possible, the coloring layer containing low ratio of pigment is preferably used for the EL light emitting device. Besides, by thinning the thickness of the coloring layer, more amount of light can be obtained. Further, it is unnecessary for the coloring layer to have a sharp peak at a wavelength as a coloring layer used in a liquid crystal display device, but the coloring layer with a broad peak wavelength is rather preferred.

[0060]

In addition, by making the coloring layer contain a black pigment, external

light entering the EL light emitting device from outside can be absorbed to avoid a defect such that an observer is projected on a cathode.

[0061]

Moreover, this embodiment is characterized in that the red coloring layer is used as a shielding film for reducing a leak current of the TFT. Since the crystalline silicon film to become the channel forming region has a small absorption coefficient with respect to light with a wavelength of approximately 650 nm (red light), it is considered that the red light does not affect an increase in the leak current with respect to the red light. Therefore, in this embodiment, the red coloring layer is used for shielding light with a wavelength of approximately 550 nm (green light) and light with a wavelength of approximately 450 nm (blue light) to prevent the leak current of the TFT from increasing.

[0062]

Furthermore, an interlayer insulating film 375 formed of a resin film is formed, covering the coloring layer 373 in which the openings 374a to 374i are formed. The interlayer insulating film 375 is desirably formed thick enough to sufficiently flatten steps formed by providing the coloring layer 373, which is a thickness of 1 to 4 μm (preferably 2 to 3 μm).

[0063]

It is effective to perform Plasma treatment using CF_4 gas to a surface of the interlayer insulating film 375. This treatment can enhance the contact of a wiring to be formed later.

[0064]

Subsequently, as shown in FIG. 4A, contact holes are formed in the interlayer insulation film 375 for forming wirings 376 to 382. In this embodiment, the wirings are provided as a lamination film of a three layer structure in which titanium film with a thickness of 50 nm, an aluminum film with a thickness of 400 nm containing titanium, and a titanium film with a thickness of 100 nm are continuously formed by a sputtering method. It is needless to say that other conductive films can be used as well.

[0065]

At this time, the wirings 376 and 378 function as source wirings for a CMOS circuit, and the wiring 377 functions as a drain wiring. Further, the wiring 379 functions to electrically connect the source wiring 340 and the source region of the switching TFT, and the wiring 380 functions to electrically connect the drain wiring 341 and the drain region of the switching TFT.

[0066]

Next, a pixel electrode 383 is formed of an oxide conductive film which is transparent to visible light. In this embodiment, an oxide conductive film obtained by adding gallium oxide to zinc oxide is used as the pixel electrode 383 with a thickness of 120 nm. Besides, an oxide conductive film formed of indium oxide, zinc oxide, tin oxide, or a compound of them can be used.

[0067]

Next, as shown in FIG. 4B, a bank 384 is formed. The bank 384 can be formed by patterning an insulating film with a thickness of 10 to 400 nm containing silicon or an organic resin film. The bank 384 is formed so as to fill in between pixels (between pixel electrodes). Moreover, the bank 384 is provided for preventing an organic EL material such as a light emitting layer formed later from being in directly contact with an edge portion of the pixel electrode 383.

[0068]

Since the bank 384 is an insulating film, the deposition is required to be carried out carefully not to cause electrostatic discharge of elements. In this embodiment, carbon particles or a pigment is added into the insulating film to be the material of the bank 384 to lower resistivity, thereby the generation of static electricity is prevented. At this time, the amount of carbon particles or pigment to be added can be adjusted so that the resitivity becomes 1×10^6 to 1×10^{12} Ωm (preferably 1×10^8 to 1×10^{10} Ωm).

[0069]

Here, pre-treatment is carried out to a surface of the pixel electrode 383. In this embodiment, a whole substrate is heated at 100 to 120°C and irradiated with ultraviolet light while oxygen plasma is formed. This allows a surface of an anode to

be treated with ozone plasma. As a result of the pre-treatment, adsorbed oxygen and adsorbed moisture are removed from the surface of anode 383 to allow a work function at the surface to be increased. Furthermore, the flatness of the anode surface is improved, which is favorably made so as to have an average square roughness (Rms) of 5 nm or less (preferably 3 nm or less).

[0070]

Instead of the ozone plasma treatment, plasma treatment using a rare gas such as argon, neon, or helium can be employed.

[0071]

Next, an EL layer 385 is formed by a spin coating method. In this embodiment, a lamination of a hole injecting layer and a light emitting layer is referred to as an EL layer. That is, a lamination, which is a combination of a light emitting layer with a hole injecting layer, a hole transporting layer, a hole blocking layer, an electron transporting layer, an electron injecting layer, or an electron blocking layer, is defined as an EL layer. These layers can be an organic material or an inorganic material, and a high molecular weight material or a low molecular weight material.

[0072]

In this embodiment, polythiophene (PEDOT) is formed to have a thickness of 20 nm as a hole injecting layer. Furthermore, as a light emitting layer that emits white light, polyvinyl carbazole (PVK) is formed to have a thickness of 80 nm. Polythiophene can be applied dissolved in water, and polyvinyl carbazole can be applied dissolved in 1,2-dichloromethane. The hole injecting layer and the light emitting layer after the application undergo heat treatment within a temperature range (typically from 80 to 120°C) that causes no breakage of the EL layer, thereby volatilizing solvent to obtain thin films.

[0073]

For example, a solution can be used, which is obtained by dissolving PVK, Bu-PBD (2-(4'-tert-butylphenyl)-5-(4"-biphenyl)-1,3,4-oxadiazole), coumarin 6, DCM1 (4-dicyanomethylene-2-methyl-6-p-dimethylaminostyryl-4H-pyran), TPB (tetraphenylbutadiene), and Nile Red into the 1,2-dichloromethane.

[0074]

Besides, as a high molecular weight material which can be used as the light emitting layer that emits white light, materials disclosed in Japanese Patent Laid-Open No. 8-96959 or Japanese Patent Laid-Open No. 9-63770 can be used.

[0075]

After the EL layer 385 is formed, a cathode 386 formed of a conductive film with a low work function is formed to have a thickness of 400 nm. In this embodiment, aluminum and lithium are alloyed by co-deposition. In this way, an EL element 387 is formed which includes the pixel electrode (anode) 383, the EL layer 385, and the cathode 386.

[0076]

After forming the cathode 386, it is effective to provide a passivation film so as to completely cover the EL element 387. At this time, it is preferable to use a film with good coverage as the passivation film, such as a carbon film, in particular a DLC film. The DLC film can be deposited in the temperature range from a room temperatures to 100°C or lower, and can be easily deposited on the upper side of the EL layer 385 which is low in heat resistance. In addition, the high blocking effect against oxygen of the DLC film can prevent the EL layer 385 and the cathode 386 from being oxidized.

[0077]

Furthermore, on the cathode 386, a sealing material 388 is provided to attach a cover material 389. As the sealing material 388, an ultraviolet curable resin can be used, in which a material with a hygroscopic effect or a material with an anti-oxidizing effect is effectively provided.

[0078]

As the cover material 389, a glass substrate, a metal substrate, a ceramics substrate, or a plastic substrate (including a plastic film) can be used. On both sides or one side of the cover material 389, a carbon film, particularly a DLC film, can be effectively provided. In the case of using the plastic film as the cover material, the

DLC film can be deposited on both sides by a roll-to-roll method.

[0079]

Thus, an EL light emitting device with a structure as shown in FIG. 4B is completed. Here, the steps after forming the bank 384 to forming the 386 are effectively processed continuously using a deposition apparatus with a multi-chamber system (or an in-line system) without exposure to the atmosphere. However, in forming the EL layer by the spin coating method, the treatment can be carried out in a deoxidized nitrogen atmosphere or a noble gas atmosphere.

[0080]

Here, each TFT is explained. A driving circuit is configured with a CMOS circuit as a basic unit in which a p-channel TFT 401 and an n-channel TFT 402 are complementarily combined. Note that the driving circuit here includes a shift register, a buffer, a level shifter, a latch, a sampling circuit (including a transfer gate), a D/A converter or the like.

[0081]

An active layer of the p-channel TFT 401 includes a source region 411, a drain region 412, and a channel forming region 413. At this time, each of the source region 411 and the drain region 412 is provided so as to overlap the first gate electrode 335a with the gate insulating film 308 interposed therebetween.

[0082]

Moreover, an active layer of the n-channel TFT 402 includes a source region 414, a drain region 415, n-type impurity regions (b) 416 and 417, n-type impurity regions (c) 418 and 419, and a channel forming region 420. At this time, each of the n-type impurity regions (b) 416 and 417 is provided so as not to overlap the first gate electrode 336a with the gate insulating film 308 interposed therebetween. Each of the n-type impurity regions (c) 418 and 419 is provided so as to overlap the first gate electrode 336a with the gate insulating film 308 interposed therebetween. Each of the n-type impurity regions (c) 418 and 419 provided so as to overlap the first gate electrode 336a has an effect of suppressing hot carrier injection to effectively prevent deterioration phenomenon due to the hot carrier injection.

[0083]

Furthermore, in the pixel portion, a switching TFT 403 and a current controlling TFT 404 are formed. The drain of the switching TFT 403 is electrically connected to the gate of the current controlling TFT 404, and a switching operation of the current controlling TFT 404 is controlled via the switching TFT 403. Further, the current controlling TFT 404 controls an amount of current flowing to the EL element.

[0084]

The active layer of the switching TFT 403 includes a source region 421, a drain region 422, n-type impurity regions (b) 423 to 426, n-type impurity regions (c) 427 to 430, an isolation region 431, and channel forming regions 432 and 433. Moreover, the source region 421 is connected to the source wiring 340 via the wiring 379. Furthermore, the drain region 422 is connected to the drain wiring 341 via the wiring 380. The drain wiring 341 is connected to the gate electrode 339 of the current controlling TFT 404.

[0085]

The structure of the switching TFT 403 is basically similar to that of the n-channel TFT 402. Each of the n-type impurity regions (b) 423 to 426 is provided so as not to overlap the first gate electrodes 337a and 338a with the gate insulating film 308 interposed therebetween, and each of the n-type impurity regions (c) 427 to 430 is provided so as not to overlap the first gate electrode 3237a and 338a with the gate insulating film 308 interposed therebetween. That is, a structure which is not easily affected by the hot carrier deterioration is provided.

[0086]

In this embodiment, an n-channel TFT is used as the switching TFT 403. However, a p-channel TFT can also be used.

[0087]

Moreover, an active layer of the current controlling TFT 404 includes a source region 434, a drain region 435, and a channel forming region 436. The structure of the current controlling TFT 404 is basically similar to that of the p-channel

TFT 401. Each of the source region 434 and the drain region 435 is provided so as to overlap the first gate electrode 339a with the gate insulating film 308 interposed therebetween. In this embodiment, a p-channel TFT is used as the current controlling TFT 404. However, an n-channel TFT can also be used.

[0088]

Here, a top plan view of the pixel portion is shown in FIG. 5. In addition, a cross sectional diagram taken along A - A' in FIG. 5 is shown in FIG. 6A, a cross sectional diagram taken along B - B' is shown in FIG. 6B, and a cross sectional diagram taken along C - C' is shown in FIG. 6C. FIGS. 6A, 6B and 6C show cross sectional structures of the switching TFT 403, a storage capacitor and the current controlling TFT 404 respectively. The pixel portion shown here can be formed by the manufacturing steps shown in FIG. 2 to FIG. 4, and explanation will be made with reference to reference numerals used in FIG. 2 to FIG. 4 as required.

[0089]

First, the switching TFT 403 is explained with reference to FIG. 5 and FIG. 6A. In FIG. 5 and FIG. 6A, reference numeral 501 denotes an active layer. Details of the active layer 501 are explained with reference to FIG. 4B, therefore, the explanation is omitted here. The source wiring 340 is electrically connected to the active layer 501 via the wiring 379, and further electrically connected to the drain wiring 341 via the wiring 380.

[0090]

A gate electrode 502 is provided over the active layer 501. In the gate electrode 502, portions which overlap the active layer 501 correspond to the gate electrodes 337 and 338 shown in FIG. 2E. The gate electrode 502 is electrically connected to a gate wiring 504 at a contact portion 503.

[0091]

Next, the current controlling TFT 404 is explained with reference to FIG. 5 and FIG. 6B. In FIG. 5 and FIG. 6B, reference numeral 505 denotes an active layer. Details of the active layer 505 are explained with reference to FIG. 4B and the explanation is omitted here. The source region of the active layer 505 is electrically

connected to a wiring (current supply line) 381, and the drain region is electrically connected to a wiring 382 and a pixel electrode (anode of the EL element) 383.

[0092]

The gate electrode 339 is provided over the active layer 505. The gate electrode 339 corresponds to a portion where the drain wiring 341 overlaps the active layer 505. The drain wiring 341 is extended to be an upper electrode 506 of the storage capacitor shown in FIG. 6C. The wiring (current supply line) 381 is electrically connected to a semiconductor film 508 at a contact portion 507. The semiconductor film 508 functions as a lower electrode of the storage capacitor.

[0093]

An example of a circuit configuration of the EL light emitting device of this embodiment is shown in FIG. 7. In this embodiment, a circuit configuration for carrying out digital driving is described. In this embodiment, a source side driving circuit 701, a pixel portion 708, and a gate side driving circuit 709 are provided. A driving circuit portion in this specification is a general term including the source side processing circuit and the gate side driving circuit.

[0094]

In this embodiment, an n-channel TFT with the structure as shown in FIG. 4B is provided as a switching TFT in the pixel portion 708. This switching TFT is arranged at an intersection of a gate wiring connected to the gate side driving circuit 709, and a source wiring connected to the source side driving circuit 701. The drain of the switching TFT is electrically connected to a gate of the p-channel current controlling TFT.

[0095]

The source side driving circuit 701 is provided with a shift register 702, a buffer 703, a latch (A) 704, a buffer 705, a latch (B) 706, and a buffer 707. In an analog driving, a sampling circuit (a transfer gate) may be provided instead of the latches (A) and (B). The gate side driving circuit 709 is provided with a shift register 710 and a buffer 711.

[0096]

Though not shown, a gate side driving circuit may further be provided on the opposite side of the gate side driving circuit 709 with the pixel portion 708 put between them. In this case, the two gate side driving circuits have the same structure in which the gate wiring is shared, and even when one of them is broken, the pixel portion normally operates by a gate signal transmitted from the other one left unbroken.

[0097]

The above configuration can be easily realized by manufacturing TFTs in accordance with the manufacturing steps shown in FIG. 2 to FIG. 4. Although only constitutions of the pixel portion and the driving circuit portion are shown in this embodiment, logic circuits such as a signal separation circuit, a D/A converter, an operational amplifier, and a gamma correction circuit can be formed on the same substrate in accordance with the manufacturing steps of this embodiment. Furthermore, it is considered that a memory, a micro processor and the like can also be formed.

[0098]

Further, the EL light emitting device after the step of sealing (or encapsulating) the EL element for protection is explained with reference to FIGS. 8A and 8B. Here, reference numerals used in FIG. 7 will be referred to as required.

[0099]

FIG 8A is a top plan view showing the EL device in a state after the sealing of the EL element. Sections shown by broken lines denoted by reference numerals 701, 708, and 709 are the source side driving circuit, the pixel portion, and the gate side driving circuit, respectively. Furthermore, reference numerals 1001, 1002, and 1003 denote a cover material, a first sealing material, and a sealing member, respectively. A sealing member (not shown) is provided between inside of the cover material 1001 enclosed by the first sealing material 1002 and the substrate on which the EL element is formed.

[0100]

Reference numeral 1004 denotes a connecting wiring for transmitting signals input to the source side driving circuit 701 and the gate side driving circuit 709. The

connecting wiring 1004 receives a video signal or a clock signal from an FPC 1005 which is an external input terminal.

[0101]

Here, a cross sectional diagram is shown in FIG. 8B, which corresponds to a section taken along A - A' in FIG. 8A. In FIGS. 8A and 8B, the same reference numerals are used for denoting the same portions.

[0102]

As shown in FIG. 8B, the pixel portion 708 and the gate side driving circuit 709 are formed on a glass substrate 1006. The pixel portion 708 is formed of a plurality of pixels each including the current controlling TFT 404 and the pixel electrode 383 electrically connected to the drain of the current controlling TFT 404. The gate side driving circuit 709 is formed using a CMOS circuit in which the p-channel TFT 401 and the n-channel TFT 402 are complementarily combined.

[0103]

The pixel electrode 383 functions as an anode of the EL element. A bank 384 is formed at each end of the pixel electrode 383. The EL layer 385 and the cathode 386 of the EL element are formed on the pixel electrode 383. The cathode 386 also functions as a common wiring to all of the pixels and is electrically connected to the FPC 1005 via the connecting wiring 1004. Further, all of the elements included in the pixel portion 708 and the gate side driving circuit 709 are covered by the cathode 386.

[0104]

Moreover, the cover material 1001 is attached by the first sealing material 1002. In this case, a spacer formed of a resin film may be provided for keeping an interval between the cover material 1001 and the EL element. The inside of the first sealing material 1002 is filled with a sealing member 1007. A photo-curable resin is preferably used for the first sealing material 1002 and the sealing member 1007. In addition, it is desirable that the first sealing material 1002 be a material that transmits as little moisture and oxygen as possible. Further, the sealing member 1007 may contain a substance with a moisture-absorption effect or a substance with an anti-oxidizing

effect.

[0105]

The sealing member 1007 provided to cover the EL element also functions as an adhesive for attaching the cover material 1001. As the sealing member 1007, polyimide, acrylic, PVC (Polyvinyl Chloride), an epoxy resin, a silicone resin, PVB (Polyvinyl Butyral) or EVA (Ethylene-Vinyl Acetate) can be used.

[0106]

In this embodiment, as the cover material 1001, a glass plate, a quartz plate, a plastic plate, a ceramics plate, an FRP (Fiberglass-Reinforced Plastics) plate, a PVF (Polyvinyl Fluoride) film, a Mylar film, a polyester film or an acrylic film can be used.

[0107]

Furthermore, in this embodiment, on both faces of the cover material 1001, carbon films (specifically, DLC films) 1008a and 1008b are provided in thicknesses of 2 to 30 nm. Such carbon films play roles of preventing oxygen and moisture from entering and mechanically protecting the surfaces of the cover material 1001. It is needless to say that it is also possible to attach a polarizing plate (typically a circular polarizing plate) to the carbon film 1008a which is provided outside.

[0108]

Moreover, after the cover material 1001 is attached using the sealing member 1007, the second sealing material 1003 is provided so as to cover the side face (exposed face) of the sealing member 1007. The same material as is used for the first sealing material 1002 can be used as the second sealing material 1003.

[0109]

By sealing the EL element in the sealing member 1007 with the structure as described above, the EL element can be completely isolated from outside and it becomes possible to prevent substances such as moisture and oxygen from entering, which promote deterioration of the EL layer due to oxidation. Accordingly, the EL light emitting device with high reliability can be manufactured.

[0110]

[Embodiment 2]

In this embodiment, an example of arranging the coloring layer is described with reference to FIG. 10. FIG. 10 is a top plan view of the pixel portion. The structure of each of the pixels is the same as that described with reference to FIGS. 5 and 6A to 6C.

[0111]

In FIG. 10, reference numeral 1201 denotes a red coloring layer, 1202 denotes a green coloring layer, and 1203 denotes a blue coloring layer. Moreover, 1204 denotes a pixel for green light emission, 1205 denotes a pixel for blue light emission, and 1206 denotes a pixel for red light emission. Here, in this embodiment, the pixel 1204 for green light emission is provided with the green coloring layer 1202, the pixel 1205 for blue light emission is provided with the blue coloring layer 1203, and the red coloring layer 1201 is provided above the pixel for red light emission and each TFT. Note that the red coloring layer 1201 has an opening portion 1208 at a contact portion 1207.

[0112]

A crystalline silicon film formed as an active layer of a TFT has a characteristic that an absorption coefficient relatively to the light (red light) with a peak wavelength of approximately 650 nm is small. Therefore, it is considered effective in reducing a leak current (or an off-current) due to optical excitation of the crystalline silicon film that the crystalline silicon film is not exposed to blue light with a peak wavelength of approximately 450 nm and green light with a peak wavelength of approximately 550 nm.

[0113]

Thus, in this embodiment, such a structure is employed that the red coloring layer which absorbs green light and blue light is provided above the TFT so that the light with a wavelength of approximately 400 to 550 nm is shielded. This makes it possible to suppress defects such as an increase in leak current of the TFT due to light emitted from an EL element.

[0114]

Note that it is effective that each of the coloring layers contains a black

pigment or carbon particles. This makes external light absorbed, reducing a problem in that an observer of the image is reflected on the cathode. However, when the content is excessive, the amount of emitted light also reduces, therefore, it is desirable that the amount of the additives be 1 to 10%.

[0115]

Note that this embodiment can be implemented by combining with Embodiment 1.

[0116]

[Embodiment 3]

In Embodiment 1, the example is presented in which an EL material from which white light emission can be obtained is used as the light emitting layer included in the EL layer, and the emitted white light then passes through the red coloring layer, the green coloring layer, or the blue coloring layer to obtain red light, green light, or blue light.

[0117]

In this embodiment, the light emitting layer from which red light emission can be obtained is formed in a pixel for red light emission, the light emitting layer from which green light emission can be obtained is formed in a pixel for green light emission, and the light emitting layer from which blue light emission can be obtained is formed in a pixel for blue light emission. The red light, the green light, and the blue light emitted from the respective light emitting layers are improved in color purity by passing through the red coloring layer, the green coloring layer, and the blue coloring layer respectively.

[0118]

In this embodiment, it is required to deposit three kinds of EL materials from which red, green or blue light can be obtained, for which known materials can be used. In addition, since it is required to deposit each pixel separately, a low molecular weight EL material may be deposited by a vapor deposition method using a shadow mask, or a high molecular weight EL material may be deposited by an ink-jetting method or a printing method.

[0119]

Note that the structure of this embodiment can be implemented by freely combining with Embodiment 1 or 2. Moreover, as described in Embodiment 3, it is effective that each of the coloring layers contains a black pigment or carbon particles.

[0120]

[Embodiment 4]

In this embodiment, an example is presented, in which an EL material from which blue light emission or bluish green light emission can be obtained is used as the light emitting layer, and the red light, the green light, or the blue light are obtained by the emitted light passing through a color conversion layer.

[0121]

In the case of this embodiment, a color conversion layer for converting blue light into red light in a pixel for red light emission is formed, and a color conversion layer for converting blue light into green light in a pixel for green light emission is formed. Known color conversion layers can be used as the color conversion layers. The blue light emitted from the light emitting layer excites the color conversion layer to generate red light or green light.

[0122]

The red light and the green light emitted from the respective color conversion layers and the blue light emitted from the light emitting layer are improved in color purity by passing through the red coloring layer, the green coloring layer, and the blue coloring layer respectively.

[0123]

In this embodiment, since only the light emitting layer from which blue light emission or bluish green light emission is obtained is required to be deposited as a light emitting layer, it is preferable to employ a simple technique such as a spin coating method or a printing method. It is needless to say that the vapor deposition method can be employed as well.

[0124]

Note that the structure of this embodiment can be implemented by freely combining with Embodiment 1 or 2. Moreover, as described in Embodiment 3, it is

effective that each of the coloring layers contains a black pigment or carbon particles.

[0125]

[Embodiment 5]

In this embodiment, an EL light emitting device is presented, which has a pixel portion with a different structure from that in Embodiment 1. Note that, except for the difference in layers in which various kinds of wirings (such as a gate wiring, a source wiring, a drain wiring, or a current supply line) are formed, a TFT structure and an EL element structure are approximately the same as those in Embodiment 1. Therefore, with respect to the same parts as Embodiment 1, the reference numerals which are used in FIGS. 5 and 6A to 6C are used here.

[0126]

Here, a top plan view of a pixel portion is shown in FIG. 11. In addition, a cross sectional diagram taken along A - A' in FIG. 11 is shown in FIG. 12A, a cross sectional diagram taken along B - B' is shown in FIG. 12B, and a cross sectional diagram taken along C - C' is shown in FIG. 12C. FIG. 12A shows a cross sectional structure of a switching TFT, FIG. 12B shows a cross sectional structure of a storage capacitor, and FIG. 12C shows a cross sectional structure of a current controlling TFT. The pixel portion shown here can be formed with reference to the manufacturing steps shown in FIGS. 2 to 4.

[0127]

First, the switching TFT is described with reference to FIGS. 11 and 12A. In FIGS. 11 and 12A, reference numeral 1301 denotes an active layer. Details of the active layer 1301 are similar to those of the switching TFT described with reference to FIG. 4B, therefore, the description thereon is omitted here. A gate wiring 1302 overlaps the active layer 1301 to function as a gate electrode. A source wiring 1303 and a drain wiring 1304 are connected to the active layer 1301, and a drain wiring 1303 is connected to a gate wiring 1305 of the current controlling TFT.

[0128]

Next, the current controlling TFT is described with reference to FIGS. 11 and 12B. Note that, the current controlling TFT has a structure in which two TFTs are

connected in parallel, one of which is described here. In FIGS. 11 and 12B, reference numeral 1306 denotes an active layer. Since details of the active layer 1306 are similar to those of the switching TFT described in FIG. 4B, the description thereon is omitted here. A source region of the active layer 1306 is connected to a current supply line 1307, and a drain region is electrically connected to a pixel electrode (an anode of the EL element) 1309 via a drain wiring 1308.

[0129]

In addition, the gate wiring 1305 of the current controlling TFT also serves as an upper electrode 1311 of a storage capacitor 1310 shown in FIG. 12C directly below the current supplying line 1307. Here, the current supply line 1307 is electrically connected to a semiconductor film 1312 and the semiconductor film 1212 functions as a lower electrode of the storage capacitor 1310. When the structure of this embodiment is employed, the storage capacitor 1310 is completely overlapped with the current supply line 1307. Therefore, an effective light emitting area of the pixel is not narrowed.

[0130]

Next, an erasing TFT is described. In the pixel of this embodiment, an erasing TFT 1313 which has the same structure as that of the switching TFT is formed. In an active layer 1314 of the erasing TFT 1313, a source region is connected to the current supply line 1307, and a drain region is electrically connected to the gate wiring 1305 of the current controlling TFT with a drain wiring 1315 interposed therebetween. Note that since the structure of the active layer 1314 is similar to that of the switching TFT, the description thereon is omitted here.

[0131]

Moreover, a gate wiring of the erasing TFT (hereinafter referred to as an erasing gate wiring) 1316 is formed in parallel to the gate wiring 1302 of the switching TFT.

[0132]

When a signal which turns on the erasing TFT 1313 is input to the erasing gate wiring 1316, the gate wiring 1305 of the current controlling TFT is forced to have

the same potential as that of the current supply line 1307. That is, since the current controlling TFT is turned off, a current supply to the EL element 387 stops, thus the light emission thereof stops and the pixel emits no light.

[0133]

In this manner, by forming the erasing TFT 1313, the pixel can be forcibly turned off and a controllability of lighting period of the pixel is enhanced. That is, in an image display by a time gray scale method, it becomes possible to easily increase the number of the gray scale levels. Note that, for an EL light emitting device using such an erasing TFT, Japanese Patent Application No. Hei 11-338786 can be referred to.

[0134]

Further, the structure of this embodiment can be implemented by freely combining with any one of the structures of Embodiments 2 to 4.

[0135]

[Embodiment 6]

In this embodiment, an example of manufacturing an EL light emitting device by different manufacturing steps from Embodiment 1 is described with reference to FIG. 13. Note that, since this embodiment is different from Embodiment 1 only in some of the manufacturing steps, the reference numerals used in Embodiment 1 are referred to as required.

[0136]

First, in accordance with the manufacturing steps in Embodiment 1, steps up to FIG. 2E are carried out. In this embodiment, however, the adding step of an n-type impurity element shown in FIG. 2C is omitted. Thus, a state of FIG. 13A is obtained.

[0137]

Next, as shown in FIG. 13B, after the resist masks 311a to 311e are removed, the semiconductor film is added an n-type impurity element (in this embodiment, phosphorus). Note that the adding step of the n-type impurity element here can be carried out under a similar condition as that of the adding step shown in FIG. 3A in Embodiment 1.

[0138]

In this manner, n-type impurity regions (b) 601 to 609 and n-type impurity regions (c) 610 to 619 are formed. Note that for the concentration of the n-type impurity element contained in the n-type impurity regions (b) 601 to 609 and the n-type impurity regions (c) 610 to 619, Embodiment 1 can be referred to.

[0139]

Next, resist masks 620a to 620e are formed and an n-type impurity element (in this embodiment, phosphorus) is added similarly to the adding step shown in FIG. 2C in Embodiment 1. Thus, n-type impurity regions (a) 621 to 629 are formed. Note that for the concentration of the n-type impurity element contained in the n-type impurity regions (a) 621 to 629, Embodiment 1 (FIG. 13C) can be referred to.

[0140]

At this time, portions covered with the resist masks 620a to 620e in each of the n-type impurity regions (b) 601 to 609 function as LDD (Light-Doped Drain) regions later. Since the length of the n-type impurity regions (b) (LDD length) that function later as the LDD regions can be freely adjusted by the resist masks 620a to 620e, this embodiment is characterized by the superior controllability of the LDD length.

[0141]

Next, the resist masks 620a to 620e are removed and a resist mask 630 is formed. Then, a p-type impurity element (in this embodiment, boron) is added similarly to the adding step in FIG. 3B in Embodiment 1. Thus, p-type impurity regions (a) 631 to 634 are formed. Note that for the concentration of the p-type impurity element contained in the p-type impurity regions (a) 631 to 634, Embodiment 1 (FIG. 13D) can be referred to.

[0142]

Thereafter, the EL light emitting device can be manufactured in accordance with the subsequent steps of the activation step shown in FIG. 3C in Embodiment 1. Moreover, the structure of the completed TFT is approximately the same as that of Embodiment 1, thus the description of Embodiment 1 can be referred to. Note that this embodiment can be implemented by freely combining with any of the structures of

Embodiments 1 to 5.

[0143]

[Embodiment 7]

In this embodiment, description is made with reference to FIG. 14 on an example of manufacturing the EL light emitting device by different manufacturing steps from Embodiment 1. Note that since this embodiment is different from Embodiment 1 only in some of the manufacturing steps, the reference numerals used in Embodiment 1 are referred to as required.

[0144]

First, in accordance with the manufacturing steps in Embodiment 1, steps up to FIG. 2E are carried out. In this embodiment, however, the step of adding an n-type impurity element shown in FIG. 2C is omitted. Thus, a state shown in FIG. 14A is obtained.

[0145]

Next, as shown in FIG. 14B, after the resist masks 311a to 311e are removed, an n-type impurity element (in this embodiment, phosphorus) is added. Note that the step of adding the n-type impurity element here can be carried out under a similar condition as that of the adding step shown in FIG. 3A in Embodiment 1.

[0146]

In this manner, n-type impurity regions (b) 601 to 609 and n-type impurity regions (c) 610 to 619 are formed. Note that for the concentration of the n-type impurity element contained in the n-type impurity regions (b) 601 to 609 and the n-type impurity regions (c) 610 to 619, Embodiment 1 can be referred to.

[0147]

Next, with the gate electrodes 335 to 339 as masks, the semiconductor film is added with an n-type impurity element (in this embodiment, phosphorus) similarly to the adding step shown in FIG. 2C in Embodiment 1. Thus, n-type impurity regions (a) 701 to 709 are formed. Note that for the concentration of the n-type impurity element contained in the n-type impurity regions (a) 701 to 709, Embodiment 1 (FIG. 14C) can be referred to.

[0148]

Next, a resist mask 710 is formed, and a p-type impurity element (in this embodiment, boron) is added similarly to the adding step as shown in FIG. 3B in Embodiment 1. Thus, p-type impurity regions (a) 711 to 714 are formed. Note that for the concentration of the p-type impurity element contained in the p-type impurity regions (a) 711 to 714, Embodiment 1 (FIG. 14D) can be referred to.

[0149]

Thereafter, the EL light emitting device can be manufactured in accordance with the subsequent steps of the activation step of Embodiment 1 shown in FIG. 3C. Moreover, the structure of the completed TFT is approximately the same as that of Embodiment 1, therefore, the description in Embodiment 1 can be referred to. Note that this embodiment can be implemented by freely combining with any structures of Embodiments 1 to 5.

[0150]

[Embodiment 8]

While a resin film is used as the interlayer insulating film 375 in Embodiment 1, an insulating film containing silicon, specifically, a silicon oxide film is used in this embodiment. In the case of this embodiment, when the steps up to FIG. 3B are finished, a protection film (in this embodiment, a silicon nitride oxide film) with a thickness of 100 to 200 nm is formed so as to cover the gate electrode.

[0151]

Next, the activation step is carried out similarly to FIG. 3C, and an interlayer insulating film (in this embodiment, a silicon oxide film) with a thickness of 800 nm to 1 μm is subsequently formed. In this embodiment, prior to forming the interlayer insulating film, heat treatment is carried out in an atmosphere containing 3 to 100% of hydrogen at 350 to 500°C to terminate dangling bonds in the active layer with excited hydrogen.

[0152]

After these steps, a source wiring or a drain wiring is formed over the interlayer insulating film, and then the source wiring and the drain wiring are covered

with a passivation film. In this embodiment, a silicon nitride film or a silicon nitride oxide film is used as the passivation film.

[0153]

Note that the structure of this embodiment can be implemented by freely combining with any structures of Embodiments 1 to 7.

[0154]

[Embodiment 9]

In this embodiment, description is made with reference to FIG. 9 on an example of sealing an EL element with a different structure from that of the EL display device described in Embodiment 1. Note that the same portions as those in FIG. 8 are denoted by the same reference numerals.

[0155]

In this embodiment, as a cover material 1101, a plastic film having DLC films 1102a and 1102b formed on opposite surfaces is used. When the DLC films are formed on opposite surfaces of the plastic film, a roll-to-roll method can be employed, in which a rolled plastic film is used for forming a film.

[0156]

In this embodiment, to a substrate on which elements up to the EL element are formed according to Embodiment 1, the cover material 1101 is attached using a sealing member 1103. The end portion of the cover material 1101 is sealed by a sealing material 1104. As the sealing member 1103 and the sealing material 1104 which are used in this embodiment, the materials presented in Embodiment 1 can be used.

[0157]

Note that the structure of this embodiment can be implemented by freely combining with any structures of Embodiments 1 to 8.

[0158]

[Embodiment 10]

In this embodiment, a description is made on circuit diagrams of the pixel structures shown in FIG. 5 in Embodiment 1 and FIG. 11 in Embodiment 5. Here, a

circuit diagram corresponding to FIG. 5 is shown in FIG. 15A and a circuit diagram corresponding to FIG. 11 is shown in FIG. 15B.

[0159]

In FIG. 15A, reference numeral 340 denotes a source wiring, 381 denotes a current supply line, and 504 denotes a gate wiring. These reference numerals correspond to FIG. 5. Furthermore, 1501 denotes the switching TFT shown in FIG. 6A, 1502 denotes the current controlling TFT shown in FIG. 6B, 1503 denotes the storage capacitor shown in FIG. 6C, and 1504 denotes an EL element.

[0160]

When the pixel shown in this embodiment is driven digitally, the driving method disclosed in Japanese Patent Application No. 2000-114592 can be referred to.

[0161]

Next, in FIG. 15B, reference numeral 1303 denotes a source wiring, 1307 denotes a current supply line, and 1302 denotes a gate wiring. These reference numerals correspond to FIG. 11. Furthermore, 1505 denotes the switching TFT shown in FIG. 12A, 1506 denotes the current controlling TFT shown in FIG. 12B, 1507 denotes the storage capacitor shown in FIG. 12C, 1508 denotes an EL element, and 1509 denotes an erasing TFT.

[0162]

When the pixel shown in this embodiment is driven digitally, the driving method disclosed in Japanese Patent Application No. Hei 11-338786 can be referred to.

[0163]

Note that the structure of this embodiment can be implemented by freely combining with any structures of Embodiments 1 to 9.

[0164]

[Embodiment 11]

An example of a deposition apparatus used for forming the EL element in implementing the present invention is shown in FIG. 16. Note that in this embodiment, description is made on the case in which a deposition apparatus of an in-line system is employed. In FIG. 16, reference numeral 801 denotes a loading chamber from which a

transportation of a substrate 80 is carried out. The loading chamber 801 is provided with an evacuating system 800a comprising a first valve 81, a turbo molecular pump 82, a second valve 83, and a rotary pump (an oil rotary pump) 84.

[0165]

The first valve 81 is a main valve which sometimes serves as a conductance valve or a butterfly valve is used. The second valve 83 is a fore valve and the second valve 83 is first opened for decompressing coarsely the loading chamber 801 by the rotary pump 84. Subsequently, the first valve 81 is opened and decompressed up to a high vacuum by the turbo molecular pump 82. Note that instead of the turbo molecular pump, a mechanical booster pump or a cryopump can be used. The cryopump is particularly effective for removing moisture.

[0166]

Next, reference numeral 802 denotes a pretreatment chamber which treats a surface of the anode or the cathode (in this embodiment, anode) of the EL element and the pretreatment chamber 802 is provided with an evacuating system 800b. Further, the pretreatment chamber 802 is sealed and blocked from the loading chamber 801 with an unillustrated gate. The pretreatment chamber 802 can be variously changed depending on a process for manufacturing the EL element.

[0167]

The pretreatments such as ozone plasma treatment, oxygen plasma treatment, argon plasma treatment, neon plasma treatment, helium plasma treatment or hydrogen plasma treatment can be carried out. Moreover, by providing a heater, heating simultaneously with the plasma treatment can be carried out. Furthermore, it is effective to realize an ultraviolet light irradiation by providing an ultraviolet light lamp.

[0168]

In this embodiment, the pretreatment is carried out, in which the ozone plasma treatment is carried out to a surface of an anode of an oxide conductive film while heating a substrate at 100°C to remove moisture and, at the same time, to increase a work function of the surface of the anode.

[0169]

Next, reference numeral 803 denotes a vapor deposition chamber for depositing an organic material by a vapor deposition method and is referred to as a vapor deposition chamber (A). The vapor deposition chamber (A) 803 is provided with an evacuating system 800c. Further, the vapor deposition chamber (A) 803 is sealed and blocked from the pretreatment chamber 802 with an unillustrated gate. In this embodiment, a hole injecting layer is formed in the vapor deposition chamber (A) 803.

[0170]

Next, reference numeral 804 denotes a vapor deposition chamber for depositing an organic material by a vapor deposition method and is referred to as a vapor deposition chamber (B). The vapor deposition chamber (B) 804 is provided with an evacuating system 800d. Further, the vapor deposition chamber (B) 804 is sealed and blocked from the vapor deposition chamber (A) 803 with an unillustrated gate. In this embodiment, a hole transport layer is formed in the vapor deposition chamber (B) 804.

[0171]

Next, reference numeral 805 denotes a vapor deposition chamber for depositing an organic EL material by a vapor deposition method and is referred to as a vapor deposition chamber (C). The vapor deposition chamber (C) 805 is provided with an evacuating system 800e. Further, the vapor deposition chamber (C) 805 is sealed and blocked from the vapor deposition chamber (B) 804 with an unillustrated gate. In this embodiment, a light emitting layer to emit red light is formed in the vapor deposition chamber (C) 805.

[0172]

Next, reference numeral 806 denotes a vapor deposition chamber for depositing an organic EL material by a vapor deposition method and is referred to as a vapor deposition chamber (D). The vapor deposition chamber (D) 806 is provided with an evacuating system 800f. Further, the vapor deposition chamber (D) 806 is sealed and blocked from the vapor deposition chamber (C) 805 with an unillustrated gate. In this embodiment, a light emitting layer to emit green light is formed in the

vapor deposition chamber (D) 806.

[0173]

Next, reference numeral 807 denotes a vapor deposition chamber for depositing an organic EL material by a vapor deposition method and is referred to as a vapor deposition chamber (E). The vapor deposition chamber (E) 807 is provided with an evacuating system 800g. Further, the vapor deposition chamber (E) 807 is sealed and blocked from the vapor deposition chamber (D) 806 with an unillustrated gate. In this embodiment, a light emitting layer to emit blue light is formed in the vapor deposition chamber (E) 807.

[0174]

Next, reference numeral 808 denotes a vapor deposition chamber for depositing an organic material by a vapor deposition method and is referred to as a vapor deposition chamber (F). The vapor deposition chamber (F) 808 is provided with an evacuating system 800h. Further, the vapor deposition chamber (F) 808 is sealed and blocked from the vapor deposition chamber (E) 807 with an unillustrated gate. In this embodiment, an electron transport layer is formed in the vapor deposition chamber (F) 808.

[0175]

Next, reference numeral 809 denotes a vapor deposition chamber for depositing an organic material by a vapor deposition method and is referred to as a vapor deposition chamber (G). The vapor deposition chamber (G) 809 is provided with an evacuating system 800i. Further, the vapor deposition chamber (G) 809 is sealed and blocked from the vapor deposition chamber (F) 808 with an unillustrated gate. In this embodiment, an electron injecting layer is formed in the vapor deposition chamber (G) 809.

[0176]

Next, reference numeral 810 denotes a vapor deposition chamber for depositing a conductive film to become an anode or a cathode of the EL element (in this embodiment, a metal film to become a cathode) and is referred to as a vapor deposition chamber (H). The vapor deposition chamber (H) 810 is provided with an evacuating

system 800j. Further, the vapor deposition chamber (H) 810 is sealed and blocked from the vapor deposition chamber (G) 809 with an unillustrated gate.

[0177]

In this embodiment, an Al-Li alloy film (an alloy film of aluminum and lithium) or an Al-Cs alloy film (an alloy film of aluminum and cesium) is formed in the vapor deposition chamber (H) 810 as a conductive film that becomes a cathode of the EL element. Note that, co-vapor-deposition of an element which belongs to group one or two in the periodic table and aluminum can be carried out.

[0178]

Next, reference numeral 811 denotes a sealing chamber which is provided with an evacuating system 800k. Further, the sealing chamber is sealed and blocked from the vapor deposition chamber (H) 810 with an unillustrated gate. In the sealing chamber 811, a DLC (Diamond-Like Carbon) film is formed as a passivation film for protecting the EL element from oxygen and water.

[0179]

For forming the DLC film, a sputtering method or a plasma CVD method can be employed. The DLC film which can be deposited at a temperature range from a room temperature to 100°C is preferable as a passivation film to protect the EL element with low heat resistance. Moreover, a thermal conductivity is high and a heat dissipation effect is well, therefore, an effect of restraining the EL element from thermal degradation can be also expected. Note that, it is also effective to use the DLC film formed in this embodiment as a lamination with a silicon nitride film or a silicon carbide film.

[0180]

Furthermore, fluorine or hydrogen can be added to the DLC film. In addition, by making the oxygen concentration in the DLC film 1×10^{18} atoms/cm^3 or lower, transmission rate of oxygen can be reduced.

[0181]

Finally, reference numeral 812 denotes an unloading chamber which is provided with an evacuating system 800l. The substrate on which the EL element is

formed is taken out from here.

[0182]

As described above, since the EL element is free from being exposed to the external air until the EL element is completely sealed in an enclosed space by using the deposition apparatus shown in FIG. 20, a highly reliable EL display device can be manufactured. In addition, the in-line system allows the EL display device to be manufactured with high throughput.

[0183]

Furthermore, it is effective that each of the treatment chambers, evacuating systems and transport systems in the deposition apparatus presented in this embodiment is operated by computer control. In this embodiment, a series of treatment are continuously carried out to complete an EL element, therefore, the computer control can manage from introducing the substrate to taking out of the substrate.

[0184]

Note that any structures of the EL display device presented in Embodiments 1 to 10 can be manufactured using the deposition apparatus presented in this embodiment.

[0185]

[Embodiment 12]

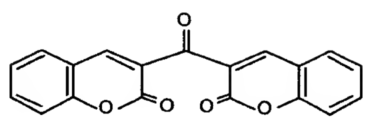
In the present invention, an external light emitting quantum efficiency can be remarkably improved by using an EL material by which phosphorescence from a triplet exciton can be employed for emitting a light. As a result, the power consumption of the EL element can be reduced, the lifetime of the EL element can be elongated and the weight of the EL element can be lightened.

Here, a report where the external light emitting quantum efficiency is improved by using the triplet exciton is presented (T. Tsutsui, C. Adachi, S. Saito, Photochemical Processes in Organized Molecular Systems, ed. K. Honda, (Elsevier Sci. Pub., Tokyo, 1991) p. 437).

The molecular formula of an EL material (coumarin pigment) reported by the above article is represented as follows.

[0186]

[Chemical Formula 1]



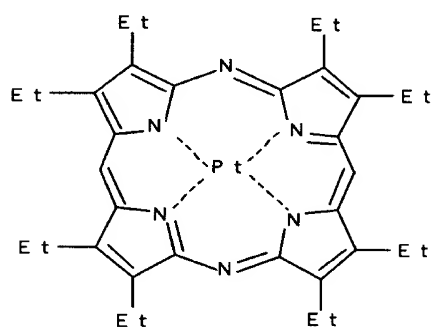
[0187]

(M. A. Baldo, D. F. O' Brien, Y. You, A. Shoustikov, S. Sibley, M. E. Thompson, S. R. Forrest, Nature 395 (1998) p.151.)

The molecular formula of an EL material (Pt complex) reported by the above article is represented as follows.

[0188]

[Chemical Formula 2]



(M. A. Baldo, S. Lamansky, P. E. Burrows, M. E. Thompson, S. R. Forrest, Appl. Phys. Lett., 75 (1999) p.4.)

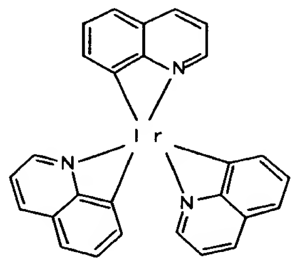
[0189]

(T. Tsutsui, M.-J. Yang, M. Yahiro, K. Nakamura, T. Watanabe, T. tsuji, Y. Fukuda, T. Wakimoto, S. Mayaguchi, Jpn. Appl. Phys., 38 (12B) (1999) L1502.)

The molecular formula of an EL material (Ir complex) reported by the above article is represented as follows.

[0190]

[Chemical Formula 3]



[0191]

As described above, if phosphorescence light emitting from a triplet exciton can be used, the external light emitting quantum efficiency can be realized by three to four times as high as that in the case of using fluorescence from a singlet exciton in principle. Note that the structure of this embodiment can be implemented by freely combining with any structure of Embodiments 1 to 11.

[0192]

[Embodiment 13]

In this embodiment, description is made with reference to FIG. 17 on specific examples of the EL element 387 shown in FIG. 4B in Embodiment 1. Note that examples of structures of the EL elements shown in this embodiment correspond to examples of an enlarged part of the EL element 387 in FIG. 4B. Known organic materials or inorganic materials can be used as materials which form EL layers in this embodiment. Further, both high molecular weight material and low molecular weight material can be used.

[0193]

First, FIG. 17A is an EL element with a structure in which a hole injecting layer 12, a hole transport layer 13, a light emitting layer 14, an electron transport layer 15, an electron injecting layer 16, and a cathode 17 are laminated on an anode (pixel electrode) 11. Note that the light emitting layer 14 can deposit three kinds of light

emitting layers corresponding to red, green and blue.

[0194]

In this embodiment, surface refinement of the anode 11 is carried out in the pretreatment chamber 802, the hole injecting layer 12 is formed in the vapor deposition chamber (A) 803, the hole transport layer 13 is formed in the vapor deposition chamber (B) 804, the light emitting layer 14 is formed in the vapor deposition chamber (C) 805 to the vapor deposition chamber (E) 807, the electron transport layer 15 is formed in the vapor deposition chamber (F) 808, the electron injecting layer 16 is formed in the vapor deposition chamber (G) 809, and the cathode 17 is formed in the vapor deposition chamber (H) 810.

[0195]

Next, FIG. 17B is an EL element with a structure in which the hole injecting layer 12, the hole transport layer 13, the light emitting layer 14, the electron injecting layer 16, and the cathode 17 are laminated on the anode (pixel electrode) 11. Note that the light emitting layer 14 can be formed by depositing three kinds of light emitting layers corresponding to red, green and blue.

[0196]

In this embodiment, surface refinement of the anode 11 is carried out in the pretreatment chamber 802, the hole injecting layer 12 is formed in the vapor deposition chamber (A) 803, the hole transport layer 13 is formed in the vapor deposition chamber (B) 804, the light emitting layer 14 is formed in the vapor deposition chamber (C) 805 to the vapor deposition chamber (E) 807, the electron injecting layer 16 is then formed in the vapor deposition chamber (G) 809 passing through the vapor deposition chamber (F) 808, and the cathode 17 is formed in the vapor deposition chamber (H) 810.

[0197]

Next, FIG. 17C is an EL element with a structure in which the hole injecting layer 12, the light emitting layer 14, the electron transport layer 15, the electron injecting layer 16, and the cathode 17 are laminated on the anode (pixel electrode) 11. Note that the light emitting layer 14 can be formed by depositing three kinds of light emitting layers corresponding to red, green and blue.

[0198]

In this embodiment, surface refinement of the anode 11 is carried out in the pretreatment chamber 802, the hole injecting layer 12 is formed in the vapor deposition chamber (A) 803, the light emitting layer 14 is then formed in the vapor deposition chamber (C) 805 to the vapor deposition chamber (E) 807 passing through the vapor deposition chamber (B) 804, the electron transport layer 15 is formed in the vapor deposition chamber (F) 808, the electron injecting layer 16 is formed in the vapor deposition chamber (G) 809, and the cathode 17 is formed in the vapor deposition chamber (H) 810.

[0199]

Next, FIG. 17D is an EL element with a structure in which the hole injecting layer 12, the light emitting layer 14, the electron injecting layer 16, and the cathode 17 are laminated on the anode (pixel electrode) 11. Note that the light emitting layer 14 can be formed by depositing three kinds of light emitting layers corresponding to red, green and blue.

[0200]

In this embodiment, surface refinement of the anode 11 is carried out in the pretreatment chamber 802, the hole injecting layer 12 is formed in the vapor deposition chamber (A) 803, the light emitting layer 14 is formed in the vapor deposition chamber (C) 805 to the vapor deposition chamber (E) 807 passing through the vapor deposition chamber (B) 804, the electron injecting layer 16 is then formed in the vapor deposition chamber (G) 809 passing through the vapor deposition chamber (F) 808, and the cathode 17 is formed in the vapor deposition chamber (H) 810.

[0201]

Next, FIG. 17E is an EL element with a structure in which the hole injecting layer 12, a cluster 18, the light emitting layer 14, the electron transport layer 15, the electron injecting layer 16, and the cathode 17 are laminated on the anode (pixel electrode) 11. Note that the light emitting layer 14 can be formed by depositing three kinds of light emitting layers corresponding to red, green and blue. Further the cluster 18 is provided for increasing the work function of the anode 11. In this embodiment,

iridium, nickel, or platinum is provided in cluster (lump).

[0202]

In this embodiment, surface refinement of the anode 11 is carried out in the pretreatment chamber 802, the cluster 18 is formed in the vapor deposition chamber (A), the hole injecting layer 12 is formed in the vapor deposition chamber (B) 804, the light emitting layer 14 is formed in the vapor deposition chamber (C) 805 to the vapor deposition chamber (E) 807, the electron transport layer 15 is formed in the vapor deposition chamber (F) 808, the electron injecting layer 16 is formed in the vapor deposition chamber (G) 809, and the cathode 17 is formed in the vapor deposition chamber (H) 810.

[0203]

Next, FIG. 17F is an EL element with a structure in which the hole injecting layer 12, the cluster 18, the light emitting layer 14, the electron injecting layer 16, and the cathode 17 are laminated on the anode (pixel electrode) 11. Note that the light emitting layer 14 can be formed by depositing three kinds of light emitting layers corresponding to red, green and blue.

[0204]

In this embodiment, surface refinement of the anode 11 is carried out in the pretreatment chamber 802, the cluster 18 is formed in the vapor deposition chamber (A), the hole injecting layer 12 is formed in the vapor deposition chamber (B) 804, the light emitting layer 14 is formed in the vapor deposition chamber (C) 805 to the vapor deposition chamber (E) 807, the electron injecting layer 16 is then formed in the vapor deposition chamber (G) 809 passing through the vapor deposition chamber (F) 808, and the cathode 17 is formed in the vapor deposition chamber (H) 810.

[0205]

As described above, even EL elements with various structures can be manufactured easily when the deposition apparatus as shown in FIG. 16 is used. Note that the structure described in this embodiment can be implemented by freely combining with any structures of Embodiments 1 to 12.

[0206]

[Embodiment 14]

The light emitting apparatus formed according to the invention as a self light emitting type is highly visible in a bright place and wide in viewing angle compared to a liquid crystal display device. Accordingly, the light emitting device of the invention may be used as a display portion of various electric devices. In such a case, the light emitting apparatus of the present invention is a passive type light emitting device but may have a large size screen by decreasing the wiring resistance, therefore, the applicable field is wide.

[0207]

Electronic devices of the present invention are: a video camera; a digital camera; a goggle type display (ahead mounted display); a car navigation system; a car audio; a notebook type personal computer; a game apparatus; a portable information terminal (such as a mobile computer, a portable telephone, a portable type game machine, or an electronic book); and an image reproducing device provided with a recording medium (specifically, a device which reproduces a recording medium such as a compact disc (CD), a laser disc (LD), or a digital versatile disc (DVD), and provided with a display portion which displays the reproduced images). Specific examples of those electronic devices are shown in FIGS. 17 and 18.

[0208]

FIG. 18A illustrates an EL display including a housing 2001, a support base 2002, and a display portion 2003. The light emitting device of the present invention can be applied to the display portion 2003. Such an EL display is a self light emitting type, therefore, a backlight is not necessary. Thus, the display portion can be thinner than that of a liquid crystal display.

[0209]

FIG. 18B illustrates a video camera including a main body 2101, a display portion 2102, a sound input portion 2103, operation switches 2104, a battery 2105, and an image receiving portion 2106. The light emitting device of the present invention can be applied to the display portion 2102.

[0210]

FIG. 18C illustrates a digital camera including a main body 2201, a display portion 2202, an eye piece portion 2203, and operation switches 2204. The light emitting device of the present invention can be used as the display portion 2202.

[0211]

FIG. 18D illustrates an image reproducing device provided with a recording medium (specifically, a DVD reproducing device), including a main body 2301, a recording medium (such as a CD, LD or DVD) 2302, operation switches 2303, a display portion (a) 2304, and a display portion (b) 2305. The display portion (a) is mainly used for displaying image information. The display portion (b) is mainly used for displaying text information. The light emitting device of the present invention can be applied to the display portion (a) and the display portion (b). Note that the image reproducing device provided with a recording medium includes a CD reproducing device, a game machine and the like.

[0212]

FIG. 18E illustrates a portable type (mobile) computer including a main body 2401, a display portion 2402, an image receiving portion 2403, operation switches 2404, and a memory slot 2405. The electro-optical device of the present invention can be applied to the display portion 2402. This portable type computer can record or reproduce information in the recording medium in which a flash memory or a nonvolatile memory are integrated.

[0213]

FIG. 18F illustrates a personal computer including a main body 2501, a housing 2502, a display portion 2503, and a keyboard 2504. The light emitting device of the present invention can be applied to the display portion 2503.

[0214]

Note that if the luminance of EL material increases in the future, the invention can be applied to a front type or a rear type projector by expanding and projecting light containing output image information with a lens or the like.

[0215]

Further, the above electronic devices often display information transmitted

through an electronic communication line such as Internet and CATV (cable TV), and particularly moving image information. An EL material, which is high in response speed is suitable for displaying moving images.

[0216]

In addition, since the light emitting device consumes power in the light emitting portion, it is preferable to display information so as to make the light emitting portion as small as possible. Accordingly, when using the light emitting device in a display portion mainly for character information, such as those in a portable information terminal, in particular a portable telephone or a car audio, it is preferable to drive to form character information by the light emitting portions while non-light emitting portions are set as a background.

[0217]

Here, FIG. 19A illustrates a portable telephone including a main body 2601, a sound output portion 2602, a sound input portion 2603, a display portion 2604, an operation switch 2605, and an antenna 2606. The light emitting device of the present invention can be applied to the display portion 2604. Note that by displaying white color characters in a black color background in the display portion 2604, the power consumption of the portable telephone can be suppressed.

[0218]

In addition, FIG. 19B illustrates a car audio including a main body 2701, a display portion 2702, and operation switches 2703 and 2704. The light emitting device of the present invention can be applied to the display portion 2702. Further, a built-in audio is shown in this embodiment, but the invention can also be applied to a stationary type car audio. Note that, by displaying white color characters in a black color background in the display portion 2704, the power consumption can be suppressed.

[0219]

As described above, the application range of the present invention is extremely wide and can be used for electronic devices in various fields. Further, the electronic device of this embodiment may be obtained by using a light emitting device in which

the structures of Embodiments 1 to 13 are freely combined.

[0220]

[Effect of the Invention]

By implementing the present invention, a TFT can be manufactured by manufacturing steps which has less photolithography steps, therefore an yield of an active matrix type light emitting device using a TFT can be improved. In addition, the manufacturing term of the light emitting device is to be shortened to reduce manufacturing cost, thereby an inexpensive light emitting device can be provided. Furthermore, an inexpensive electronic appliance can be provided by using an inexpensive light emitting device.

[Brief Description of the Drawings]

FIG. 1 shows steps of manufacturing an n-channel TFT according to the present invention.

FIG. 2 shows steps of manufacturing a pixel portion and a driving circuit.

FIG. 3 shows steps of manufacturing a pixel portion and the driving circuit.

FIG. 4 shows steps of manufacturing a pixel portion and the driving circuit.

FIG. 5 shows a top plan view of a pixel portion.

FIG. 6 shows a cross sectional view of a pixel portion.

FIG. 7 shows a circuit configuration of an EL light emitting device.

FIG. 8 shows a top plan view of an EL light emitting device and a cross sectional view of the EL light emitting device.

FIG. 9 shows a top plan view of an EL light emitting device and a cross sectional view of the EL light emitting device.

FIG. 10 shows a top plan view of a pixel portion.

FIG. 11 shows a top plan view of a pixel portion.

FIG. 12 shows a cross sectional view in a pixel portion.

FIG. 13 shows steps of manufacturing a pixel portion and the driving circuit.

FIG. 14 shows steps of manufacturing a pixel portion and the driving circuit.

FIG. 15 shows a circuit configuration of a pixel.

FIG. 16 shows a structure of an in-line system deposition apparatus.

FIG. 17 shows a structure of an EL element.

FIG. 18 shows specific examples of electronic devices.

FIG. 19 shows specific examples of electronic devices.

[Document Name] Abstract

[Summary]

[Problem] A light emitting device and an electronic device are inexpensively provided.

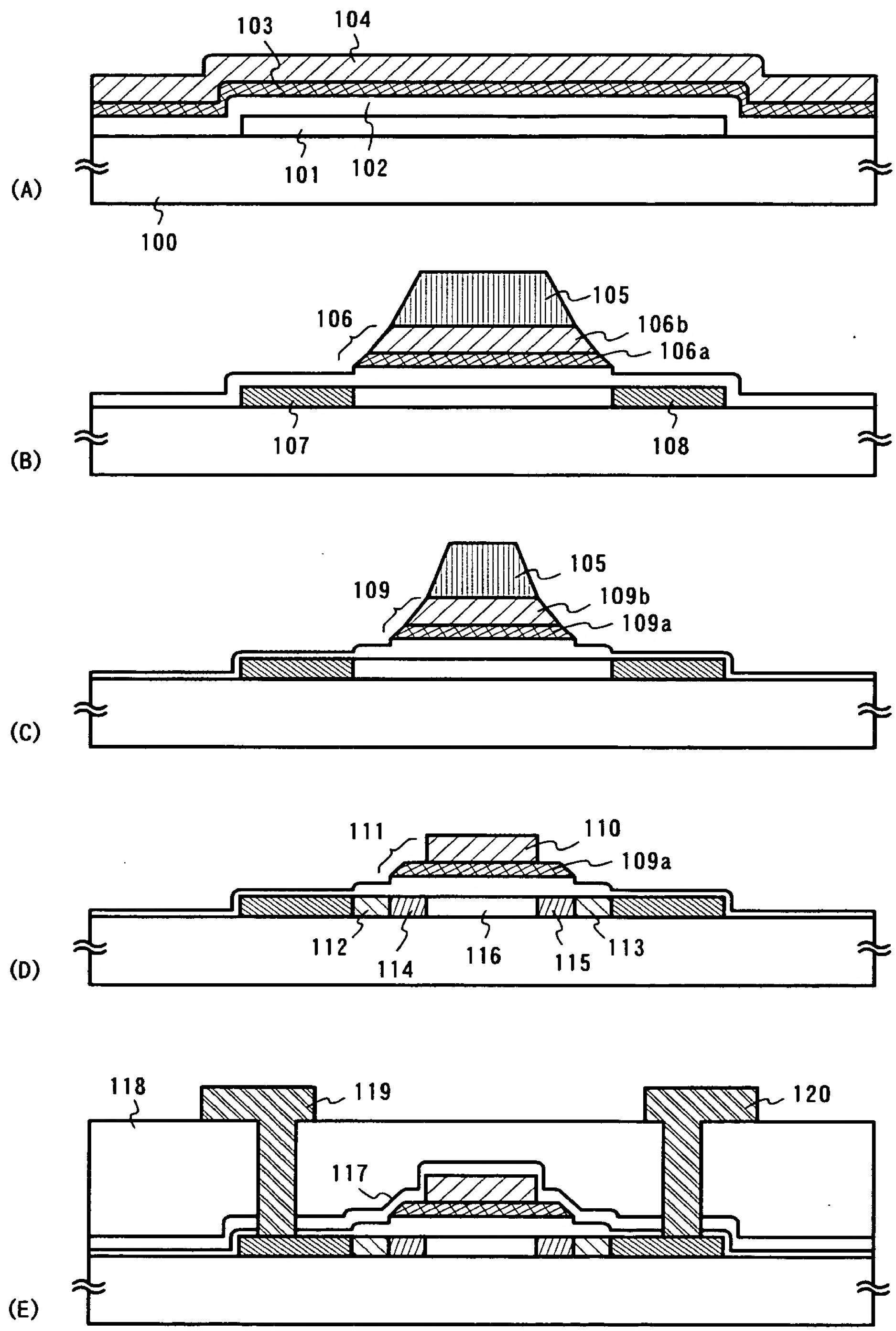
[Solving Means]

According to the present invention, the number of photolithography steps in relation to manufacturing the TFT is reduced for improving yield of the light emitting device and shortening a manufacturing term. A feature is in that a gate electrode is formed of a plurality of conductive films, and a concentration of an impurity region formed in an active layer is adjusted by making use of a selectivity of the conductive films in etching.

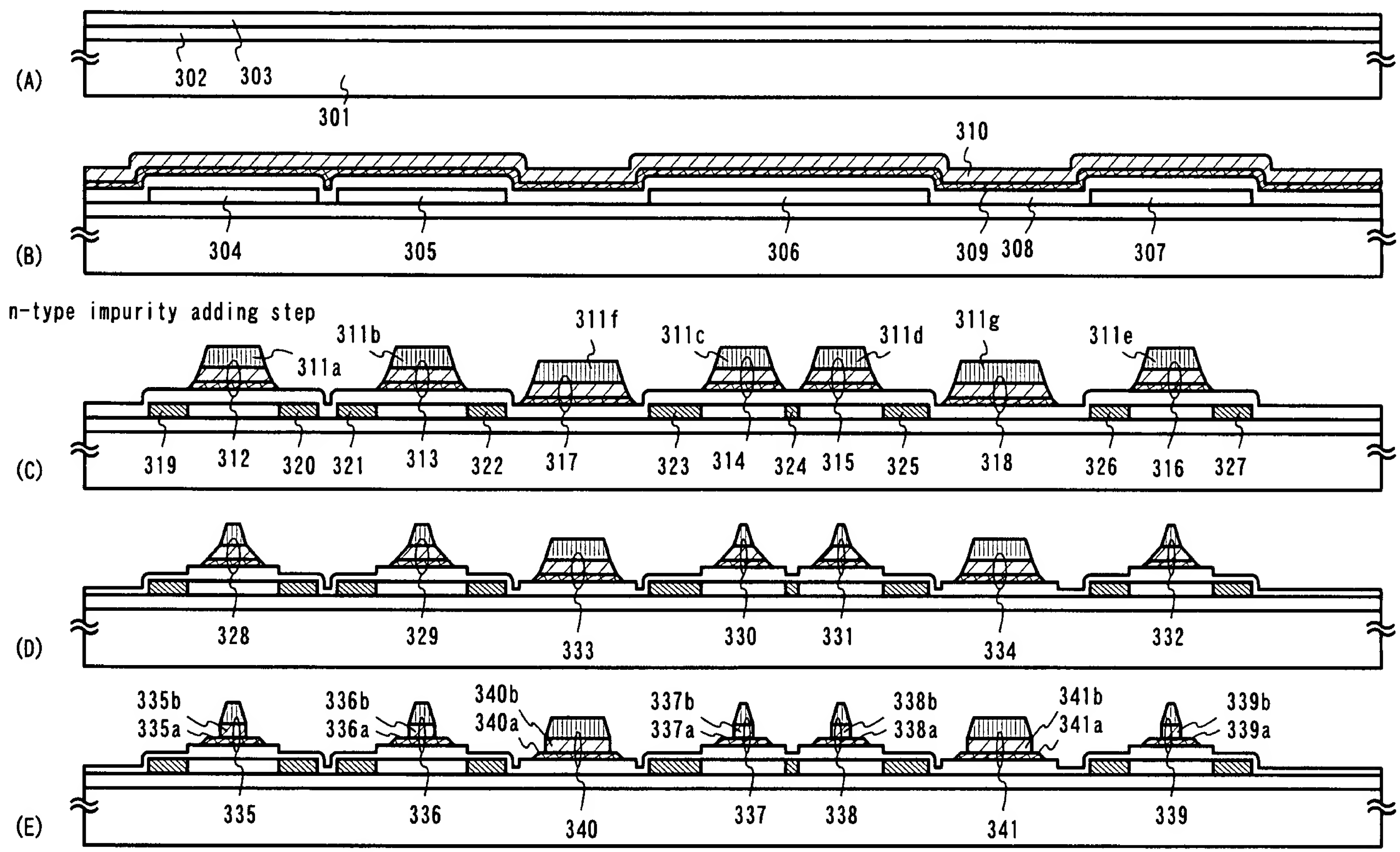
[Selected Drawing] None

【Name of Document】 Drawings

【FIG. 1】

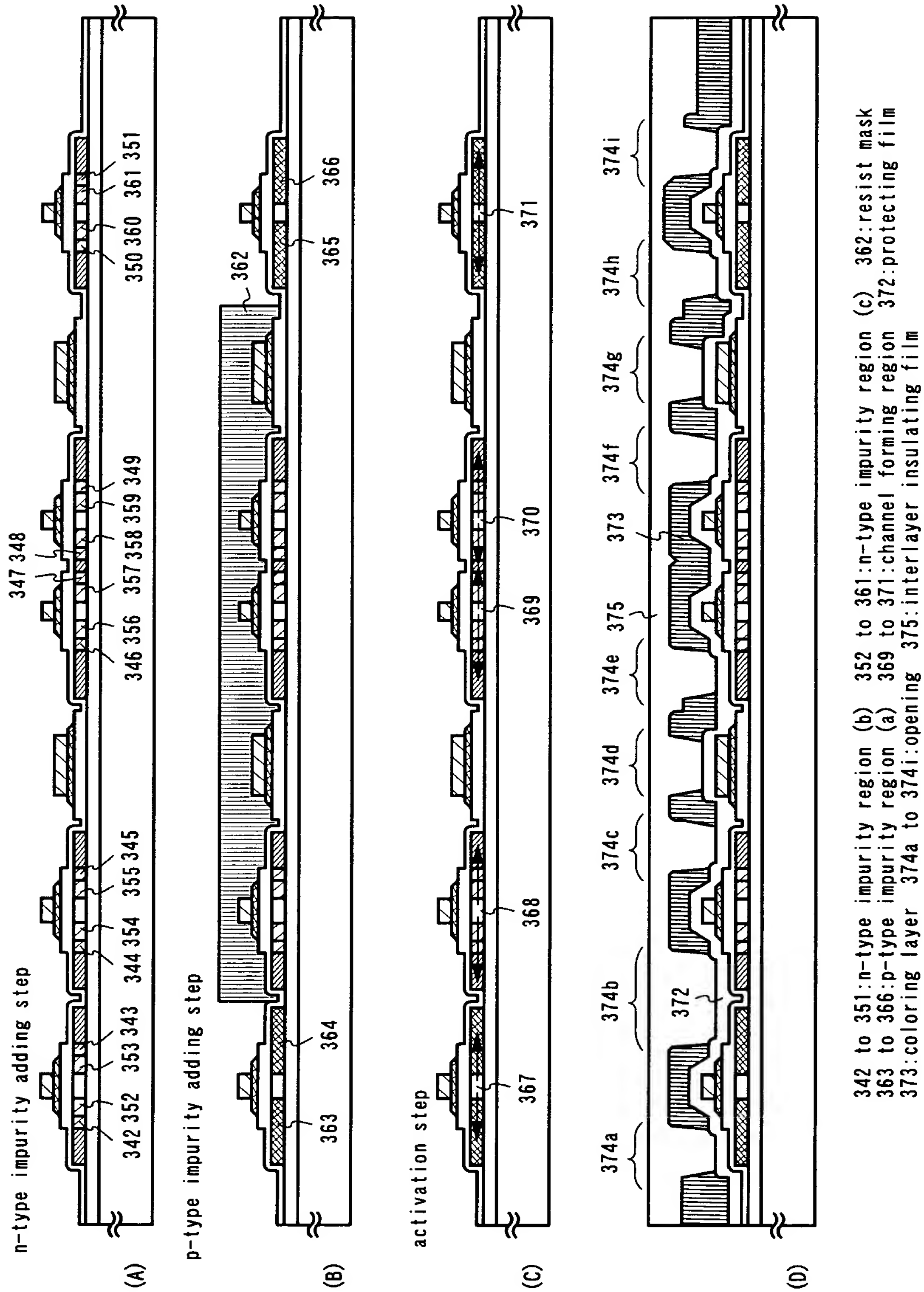


【FIG. 2】

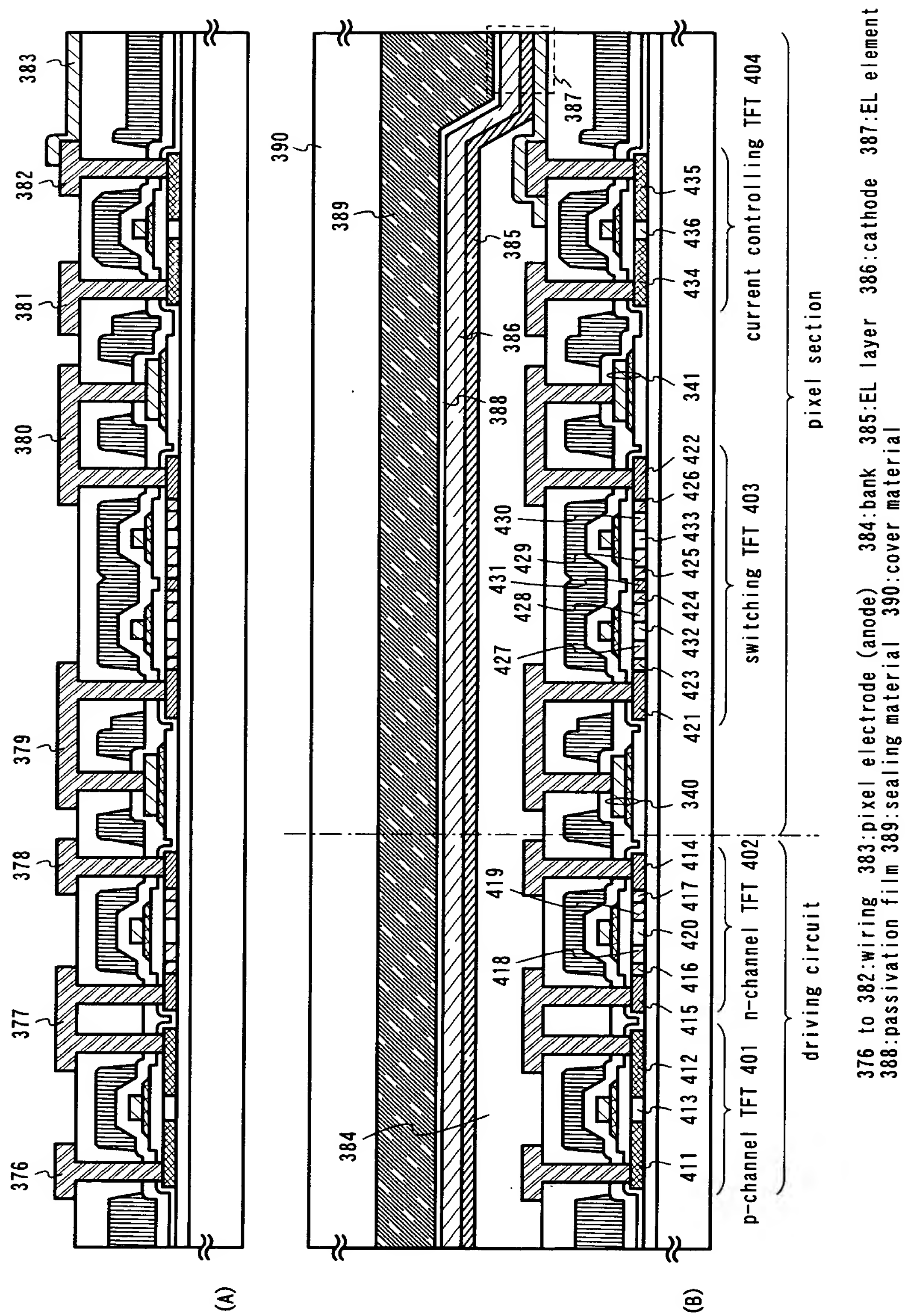


301:glass substrate 302:base film 303:polycrystalline silicon film 304 to 307:semiconductor film
308:gate insulating film 309:first conductive film 310:second conductive film 311a to 311g:resist mask
312 to 316, 328 to 332, 335 to 339:gate electrode 317, 333, 340:source wiring 318, 334, 341:drain wiring
319 to 327:n-type impurity region (a) 335a, 336a, 337a, 338a, 339a:first gate electrode
335b, 336b, 337b, 338b, 339b:second gate electrode 340a:first source wiring 340b:second source wiring
341a:first drain wiring 341b:second drain wiring

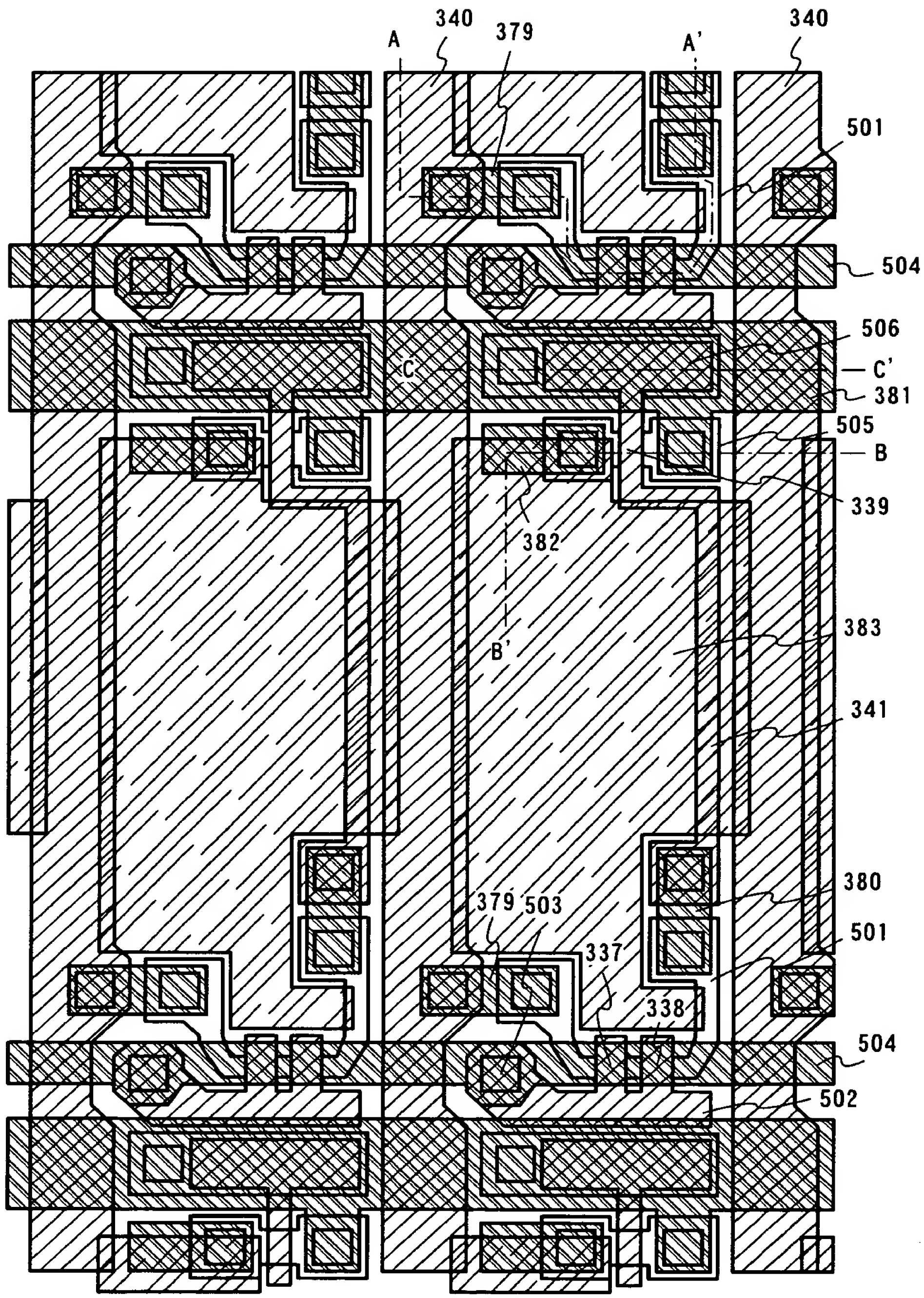
【FIG. 3】


n-type impurity adding step
(A)
342 352 353 343 344 354 355 345
346 356 357 358 359 349
347 348
350 360 361 351
p-type impurity adding step
(B)
363 364
362
365 366
activation step
(C)
367 368 369 370 371
(D)
374a 374b 374c 374d 374e 375 373 374f 374g 374h 374i
372
342 to 351:n-type impurity region (b) 352 to 361:n-type impurity region (c) 362:resist mask
363 to 366:p-type impurity region (a) 369 to 371:channel forming region 372:protecting film
373:coloring layer 374a to 374i:opening 375:interlayer insulating film

【FIG. 4】

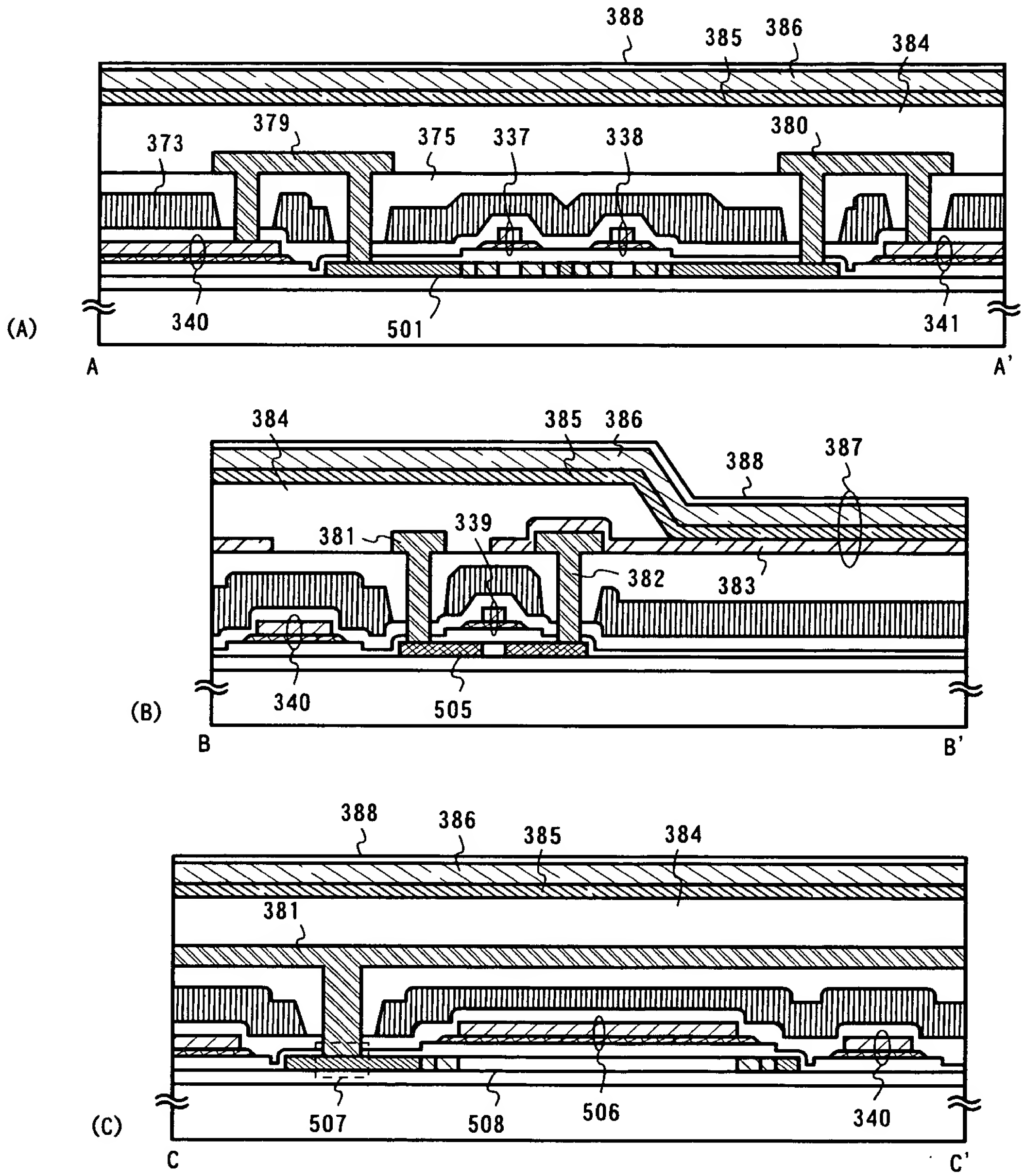

376
377
378
379
380
381
382
383
(A)
390
389
385
386
388
387
384
430
431
429
428
427
419
418
411 413 412
415 416 420 417 414
340
421 423 432 424 425 433 426 422
341
434 436 435
p-channel TFT 401
n-channel TFT 402
switching TFT 403
current controlling TFT 404
driving circuit
pixel section
(B)
376 to 382:wiring 383:pixel electrode (anode) 384:bank 385:EL layer 386:cathode 387:EL element
388:passivation film 389:sealing material 390:cover material

【FIG. 5】



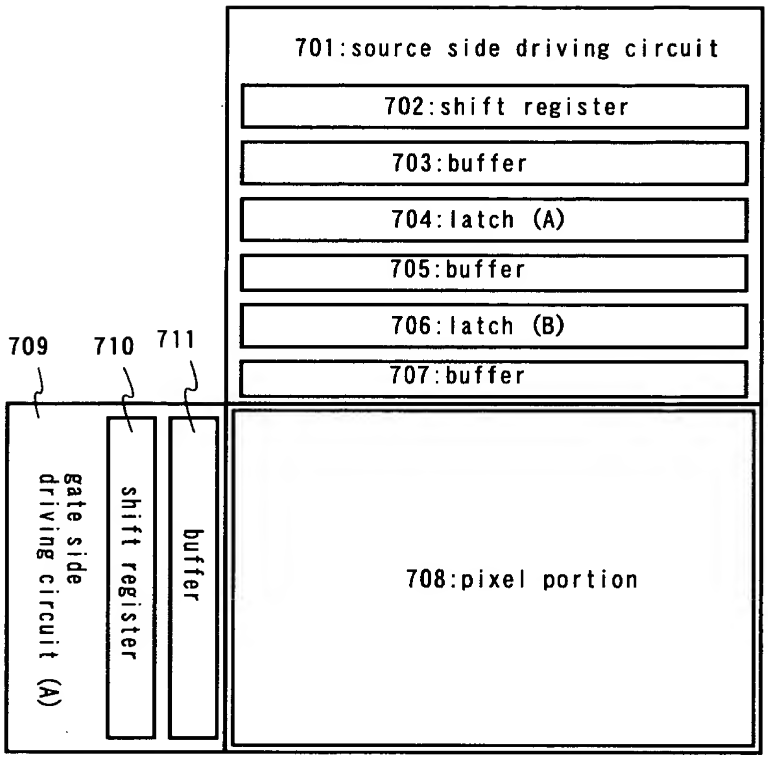
340
379
A
A'
340
501
504
506
C
C'
381
505
B
339
382
B'
383
341
380
379
503
501
337
338
504
502

【FIG. 6】

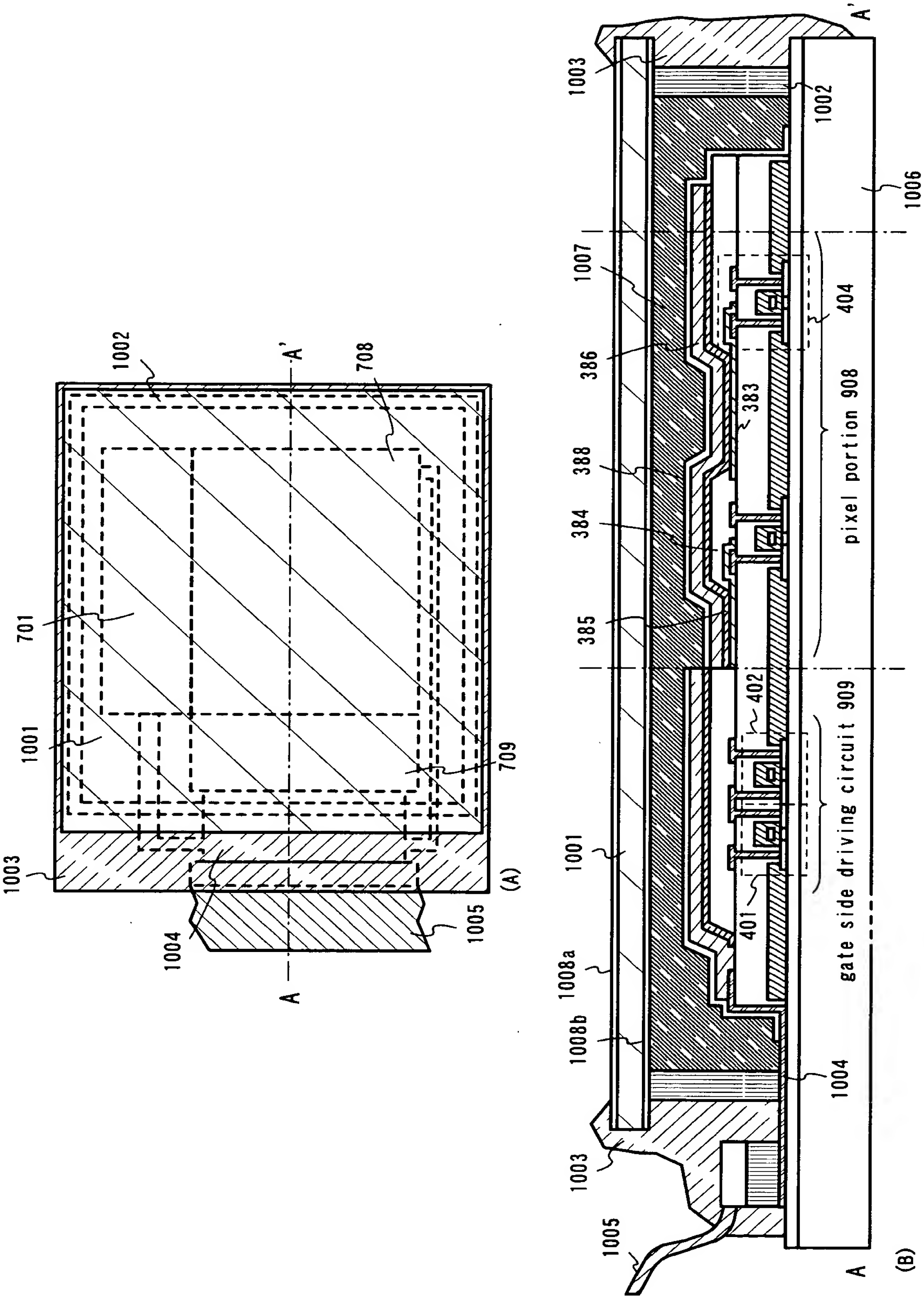


388
385
386
384
379
373
375
337
338
380
340
501
341
(A)
A
A'
384
385
386
388
387
381
339
382
383
340
505
(B)
B
B'
388
386
385
384
381
507
508
506
340
(C)
C
C'

【FIG. 7】

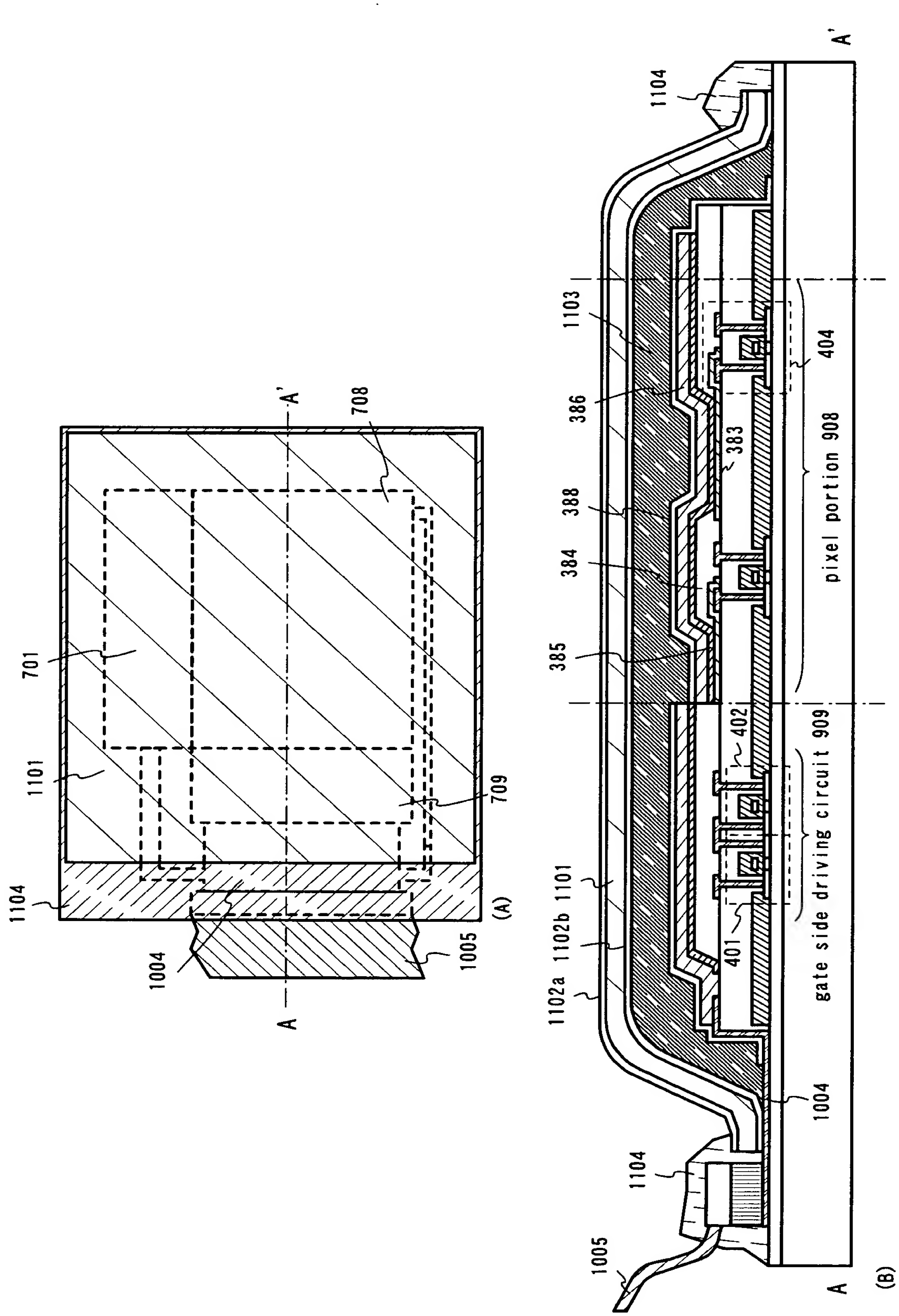

701:source side driving circuit
702:shift register
703:buffer
704:latch (A)
705:buffer
706:latch (B)
707:buffer
709
710
711
gate side driving circuit (A)
shift register
buffer
708:pixel portion

【FIG. 8】



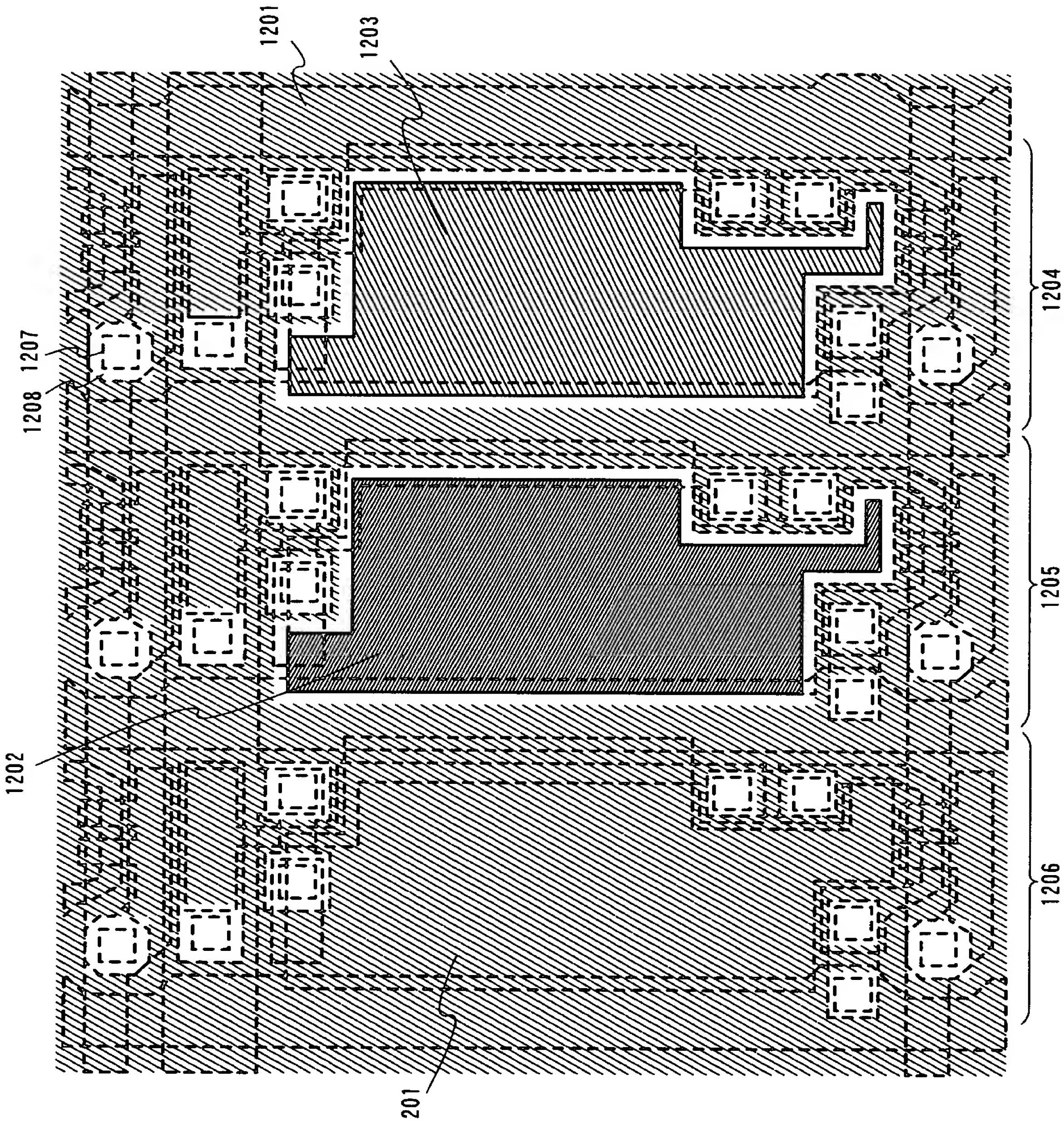
1002
708
A'
701
1001
709
1003
1004
1005
A
(A)
1003
1002
1006
1007
404
386
383
388
pixel portion 908
384
385
402
gate side driving circuit 909
1001
401
1008a
1008b
1004
1003
1005
A
A'
(B)

【FIG. 9】

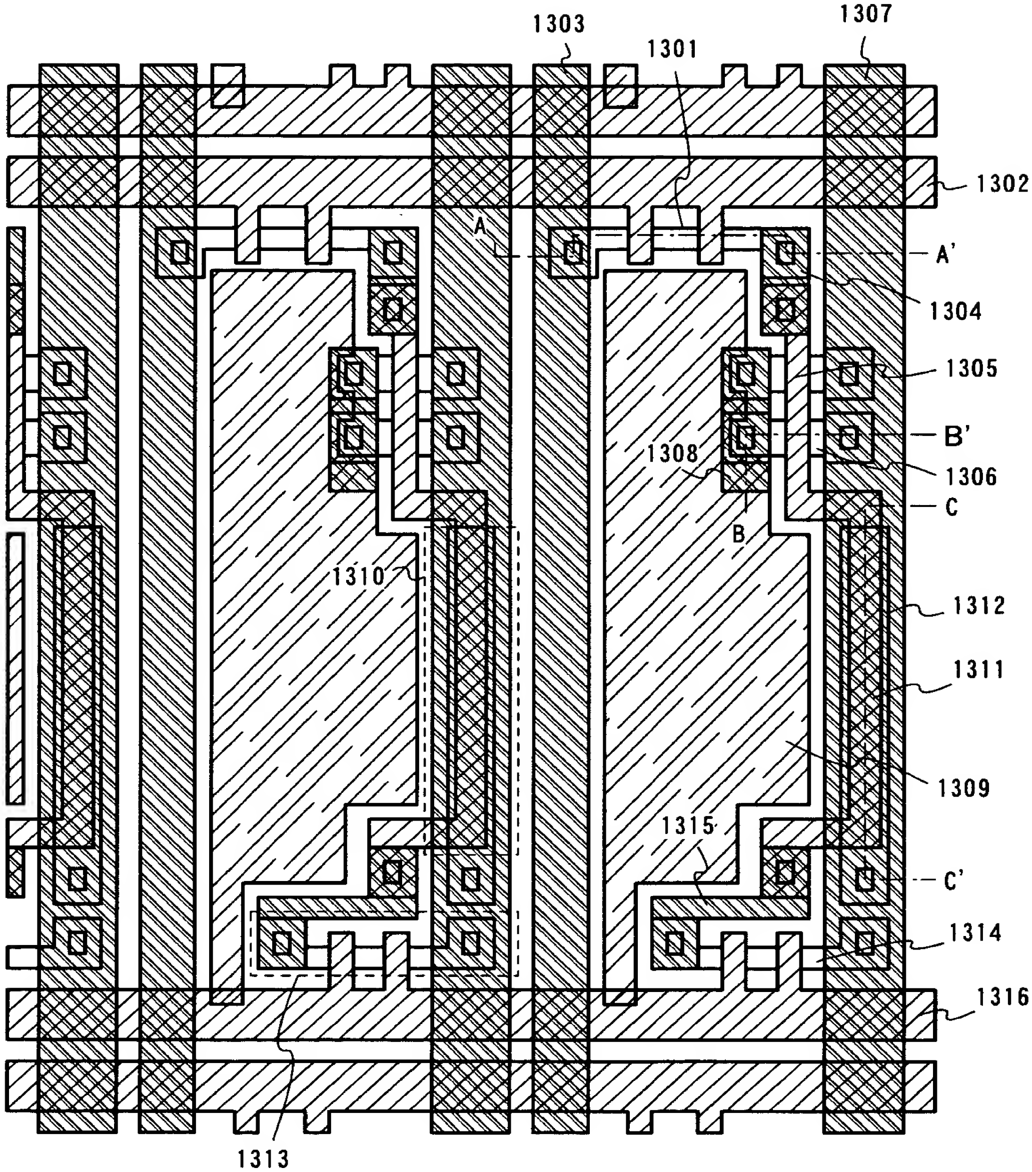


A'
708
701
1101
709
1104
1004
1005
A
(A)
1104
1103
386
388
384
385
383
404
pixel portion 908
402
gate side driving circuit 909
401
1102a
1102b
1004
1005
A
(B)

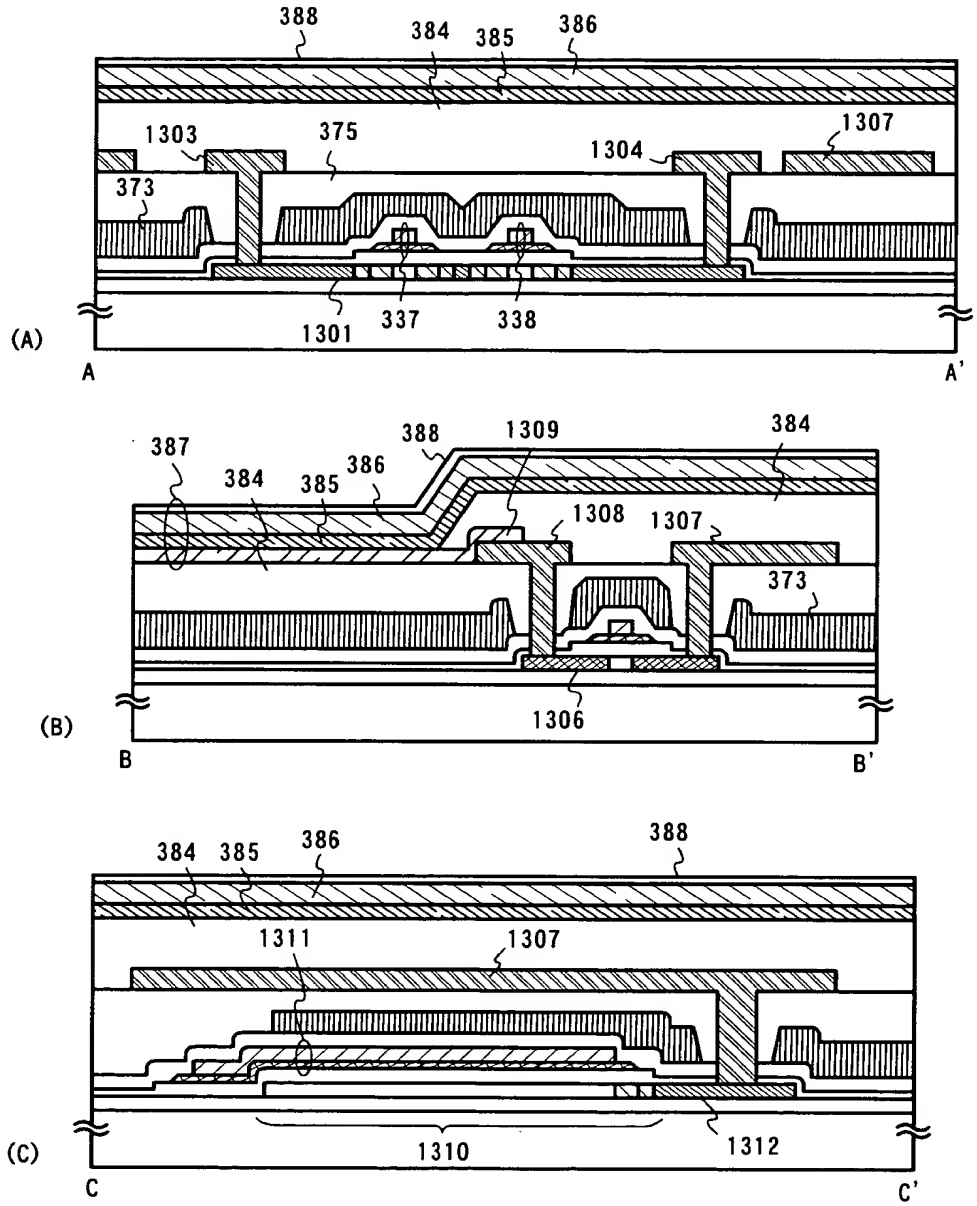
【FIG. 10】



【FIG. 11】

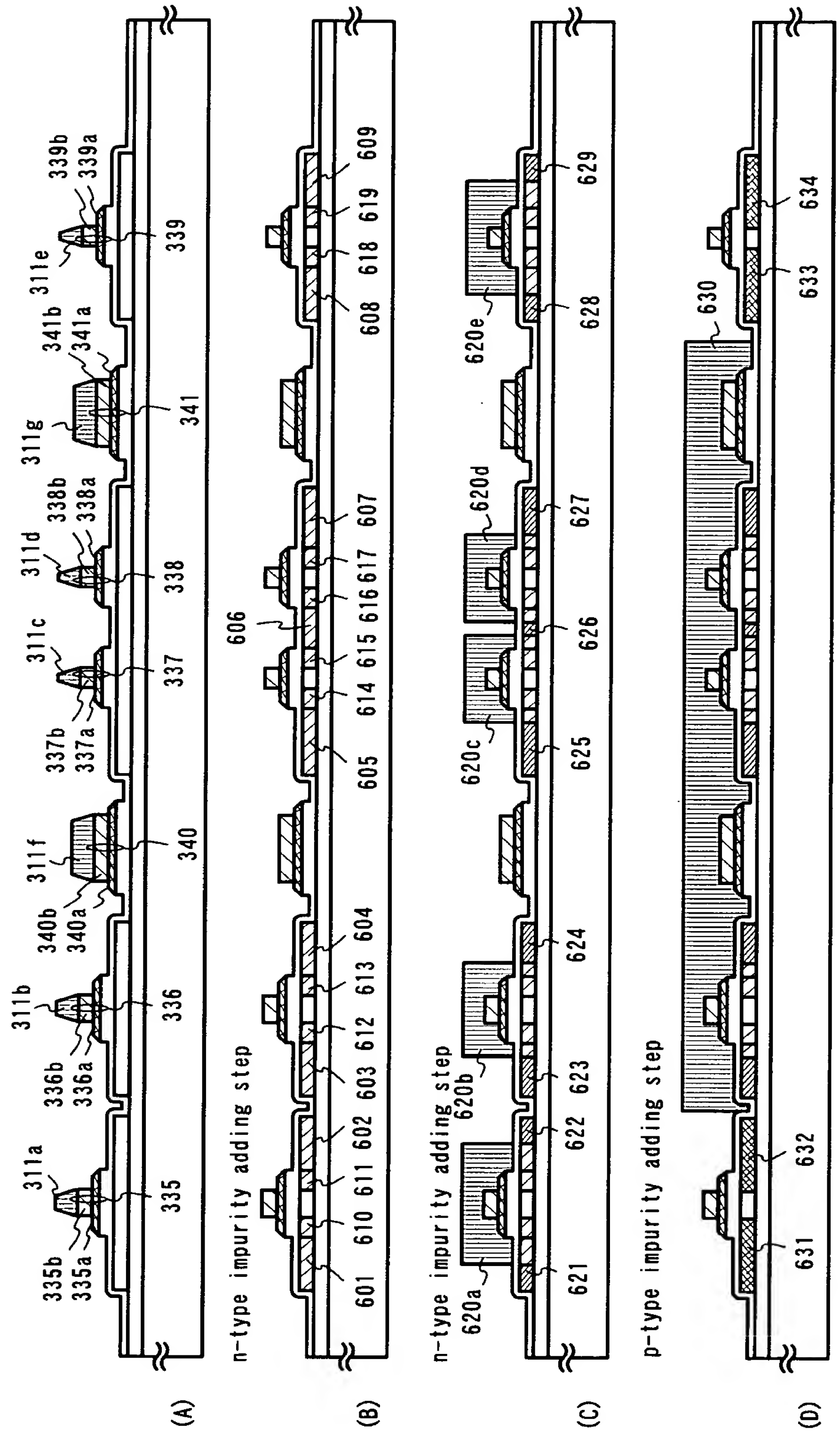

1303
1307
1301
1302
A
A'
1304
1305
B'
1308
1306
C
B
1310
1312
1311
1309
1315
C'
1314
1316
1313

【FIG. 12】



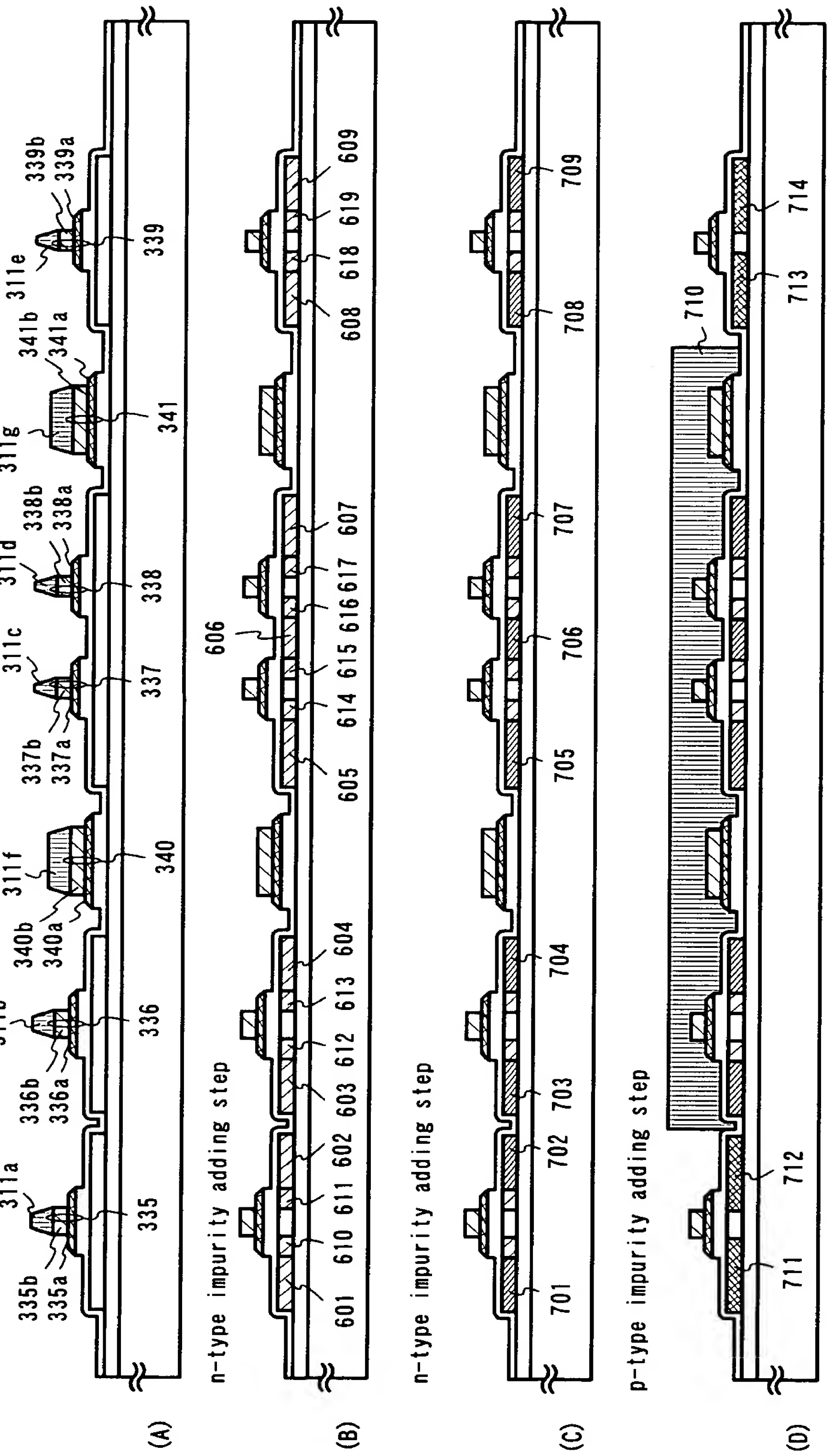
388
384
385
386
1303
375
1304
1307
373
1301
337
338
(A)
A
A'
387
388
1309
384
385
386
1308
1307
373
1306
(B)
B
B'
384
385
386
388
1311
1307
1310
1312
(C)
C
C'

【FIG. 13】



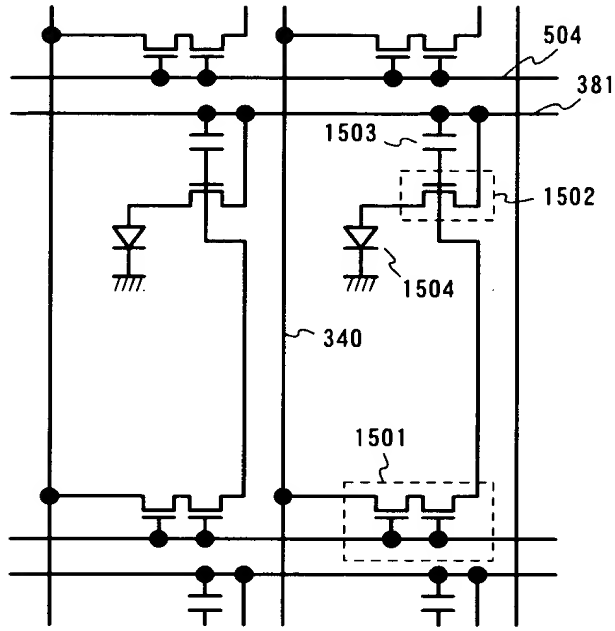
(A)
335b
335a
311a
335
336b
336a
311b
336
340b
340a
311f
340
337b
337a
311c
337
311d
338
338b
338a
311g
341
341b
341a
311e
339
339b
339a
(B)
n-type impurity adding step
601
610
611
602
603
612
613
604
605
614
615
616
617
606
607
608
618
619
609
(C)
n-type impurity adding step
620a
620b
620c
620d
620e
621
622
623
624
625
626
627
628
629
(D)
p-type impurity adding step
630
631
632
633
634

【FIG. 14】

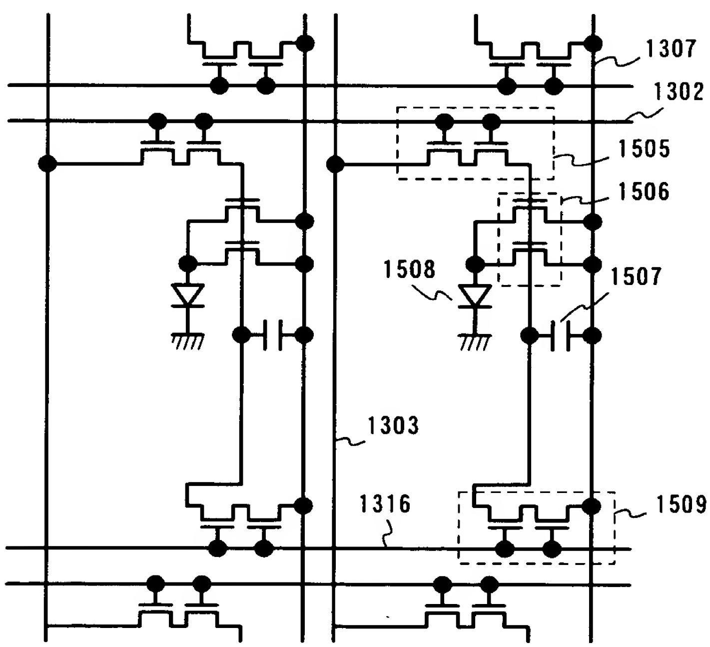


(A)
335b
335a
311a
335
336b
336a
311b
336
340b
340a
311f
340
337b
337a
311c
337
311d
338b
338a
338
311g
341b
341a
341
311e
339b
339a
339
n-type impurity adding step
(B)
601
610
611
602
603
612
613
604
605
614
615
616
617
606
607
608
618
619
609
n-type impurity adding step
(C)
701
702
703
704
705
706
707
708
709
p-type impurity adding step
(D)
711
712
710
713
714

【FIG. 15】

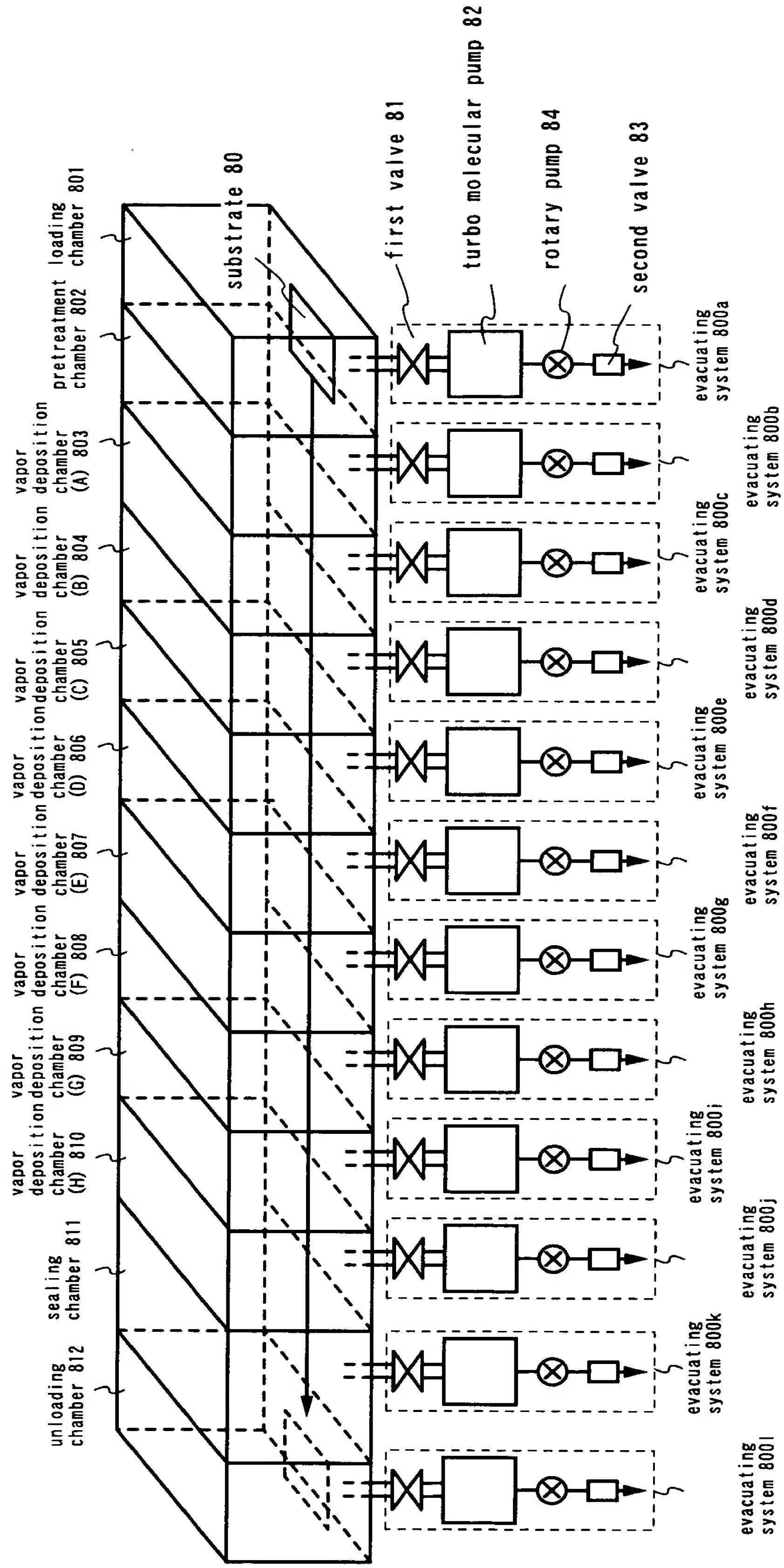

504
381
1503
1502
1504
340
1501

(A)


1307
1302
1505
1506
1508
1507
1303
1316
1509

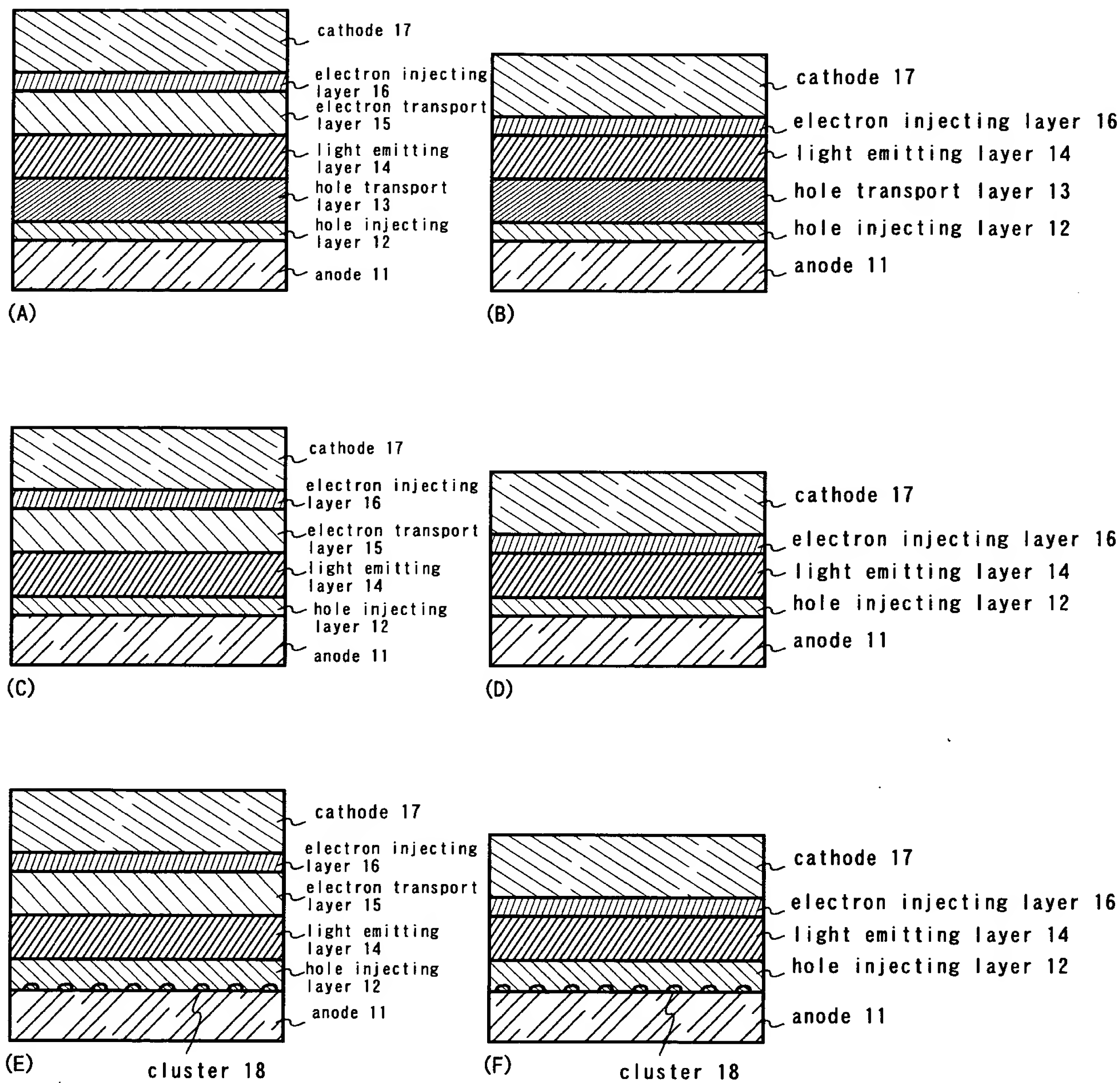
(B)

【FIG. 16】

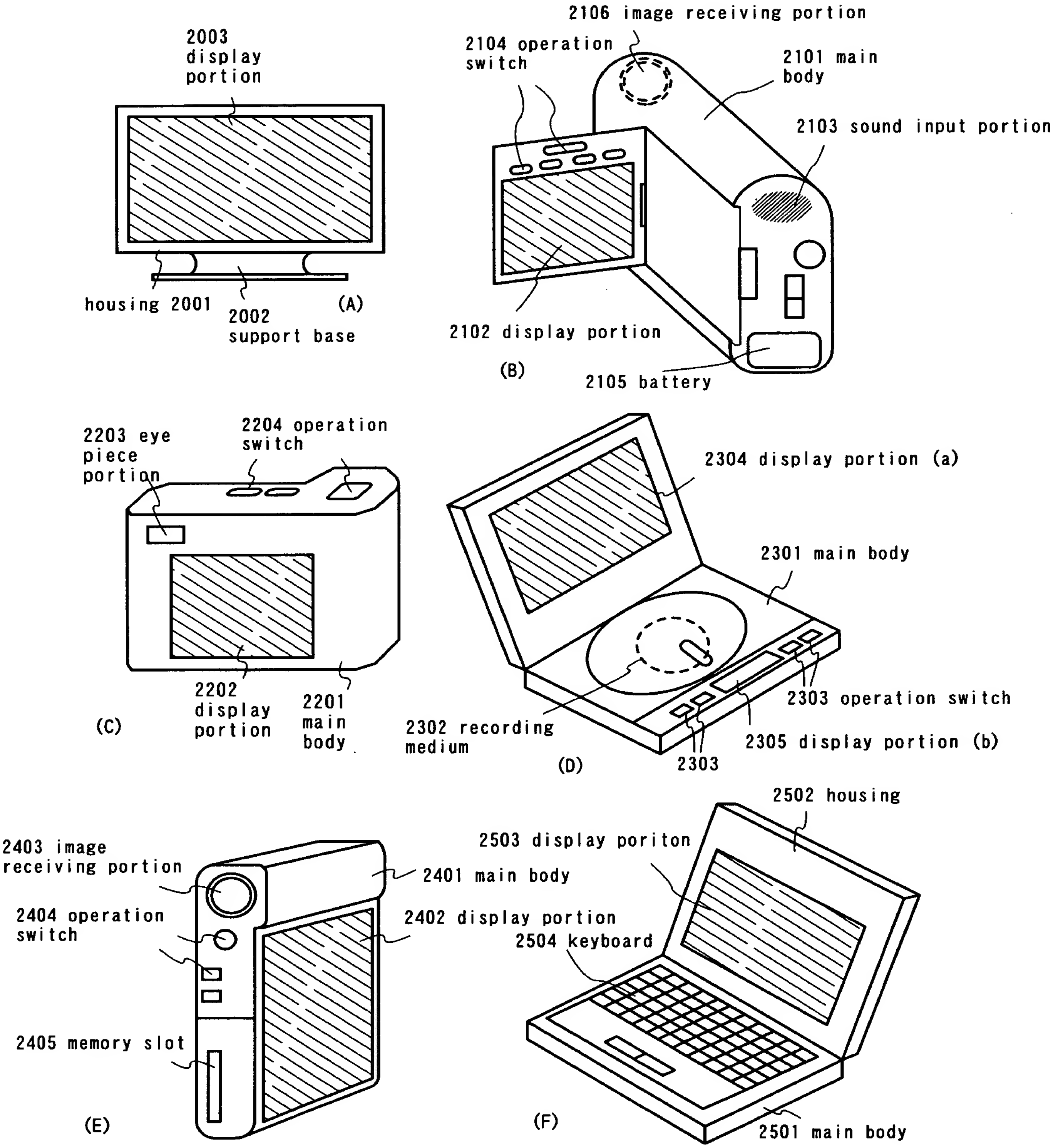


loading chamber 801
pretreatment chamber 802
vapor deposition chamber (A) 803
vapor deposition chamber (B) 804
vapor deposition chamber (C) 805
vapor deposition chamber (D) 806
vapor deposition chamber (E) 807
vapor deposition chamber (F) 808
vapor deposition chamber (G) 809
vapor deposition chamber (H) 810
sealing chamber 811
unloading chamber 812
substrate 80
first valve 81
turbo molecular pump 82
rotary pump 84
second valve 83
evacuating system 800a
evacuating system 800b
evacuating system 800c
evacuating system 800d
evacuating system 800e
evacuating system 800f
evacuating system 800g
evacuating system 800h
evacuating system 800i
evacuating system 800j
evacuating system 800k
evacuating system 800l

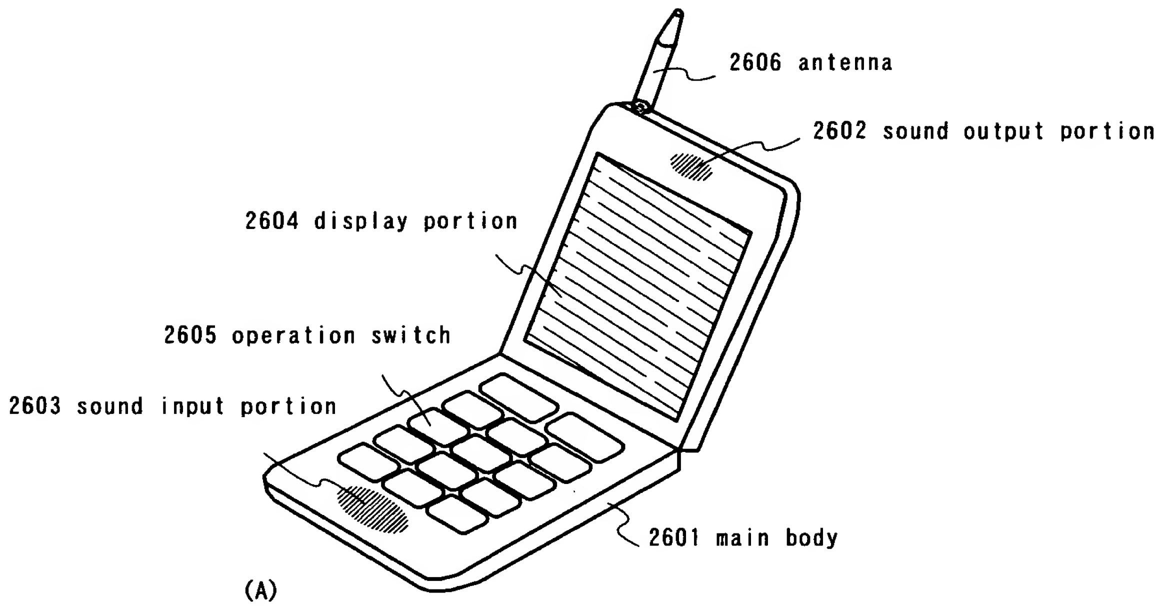
【FIG. 17】


cathode 17
electron injecting layer 16
electron transport layer 15
light emitting layer 14
hole transport layer 13
hole injecting layer 12
anode 11
(A)
cathode 17
electron injecting layer 16
light emitting layer 14
hole transport layer 13
hole injecting layer 12
anode 11
(B)
cathode 17
electron injecting layer 16
electron transport layer 15
light emitting layer 14
hole injecting layer 12
anode 11
(C)
cathode 17
electron injecting layer 16
light emitting layer 14
hole injecting layer 12
anode 11
(D)
cathode 17
electron injecting layer 16
electron transport layer 15
light emitting layer 14
hole injecting layer 12
anode 11
(E)
cluster 18
cathode 17
electron injecting layer 16
light emitting layer 14
hole injecting layer 12
anode 11
(F)
cluster 18

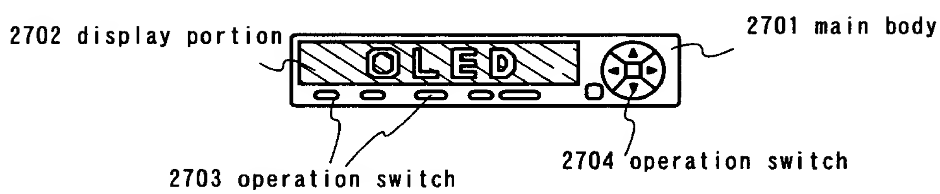
【FIG. 18】


2003 display portion
housing 2001
2002 support base
(A)
2106 image receiving portion
2104 operation switch
2101 main body
2103 sound input portion
2102 display portion
(B)
2105 battery
2203 eye piece portion
2204 operation switch
2202 display portion
2201 main body
(C)
2304 display portion (a)
2301 main body
2303 operation switch
2302 recording medium
2305 display portion (b)
(D)
2303
2502 housing
2503 display poriton
2403 image receiving portion
2401 main body
2404 operation switch
2402 display portion
2504 keyboard
2405 memory slot
(E)
(F)
2501 main body

【FIG. 19】


2606 antenna
2602 sound output portion
2604 display portion
2605 operation switch
2603 sound input portion
2601 main body

(A)


2702 display portion
OLED
2701 main body
2703 operation switch
2704 operation switch

(B)